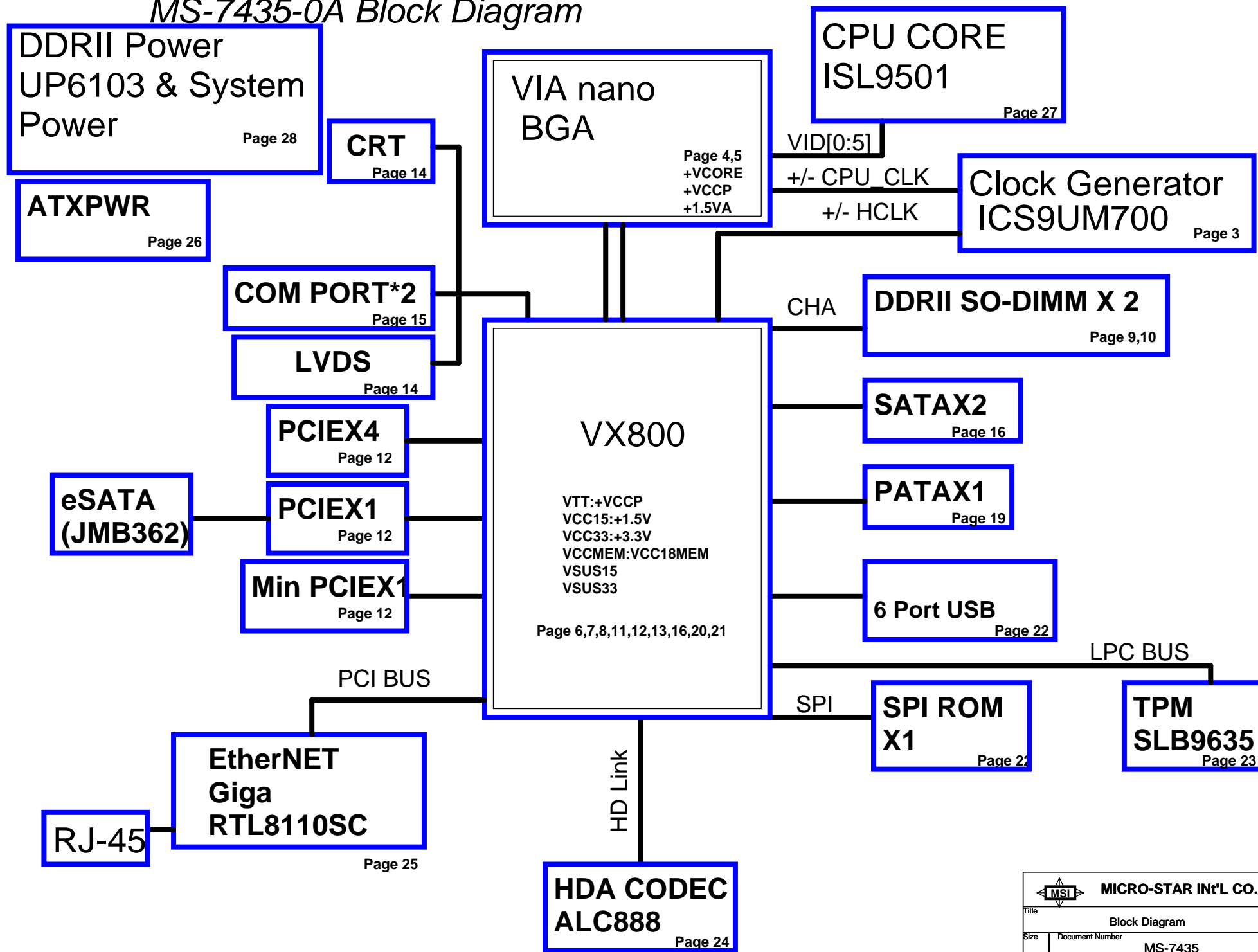
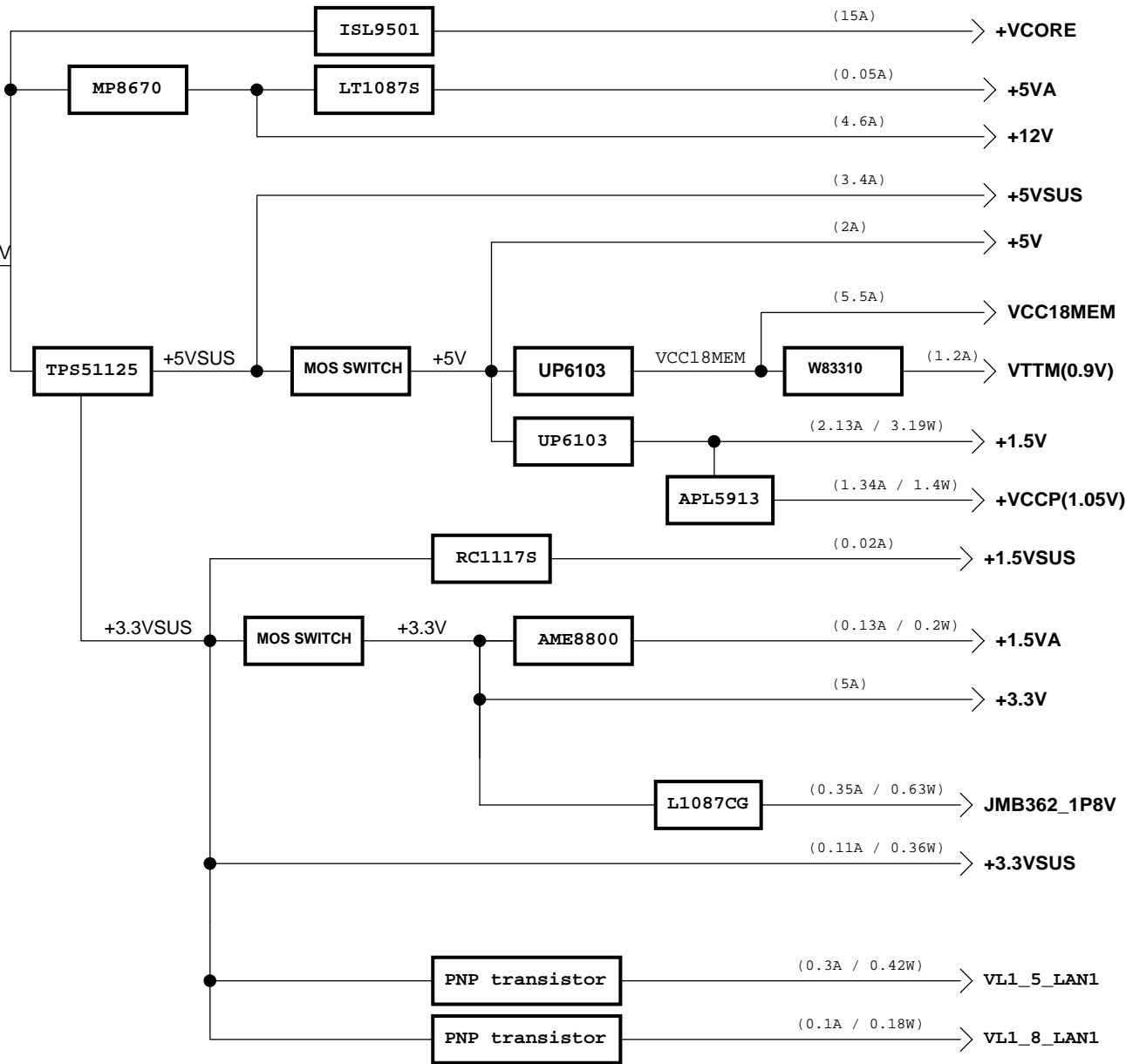
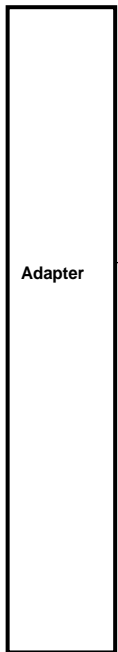


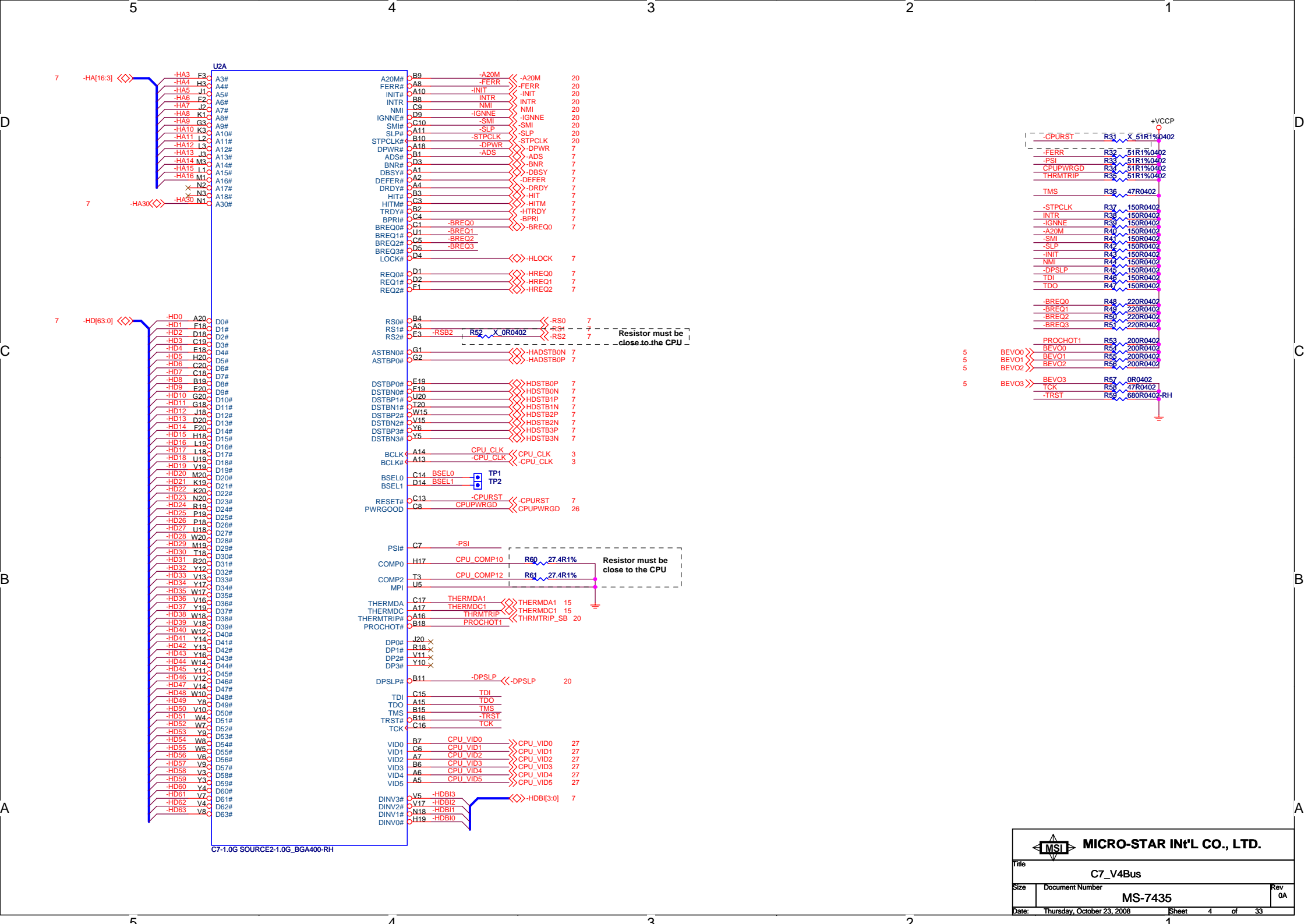
MS-7435-0A Block Diagram

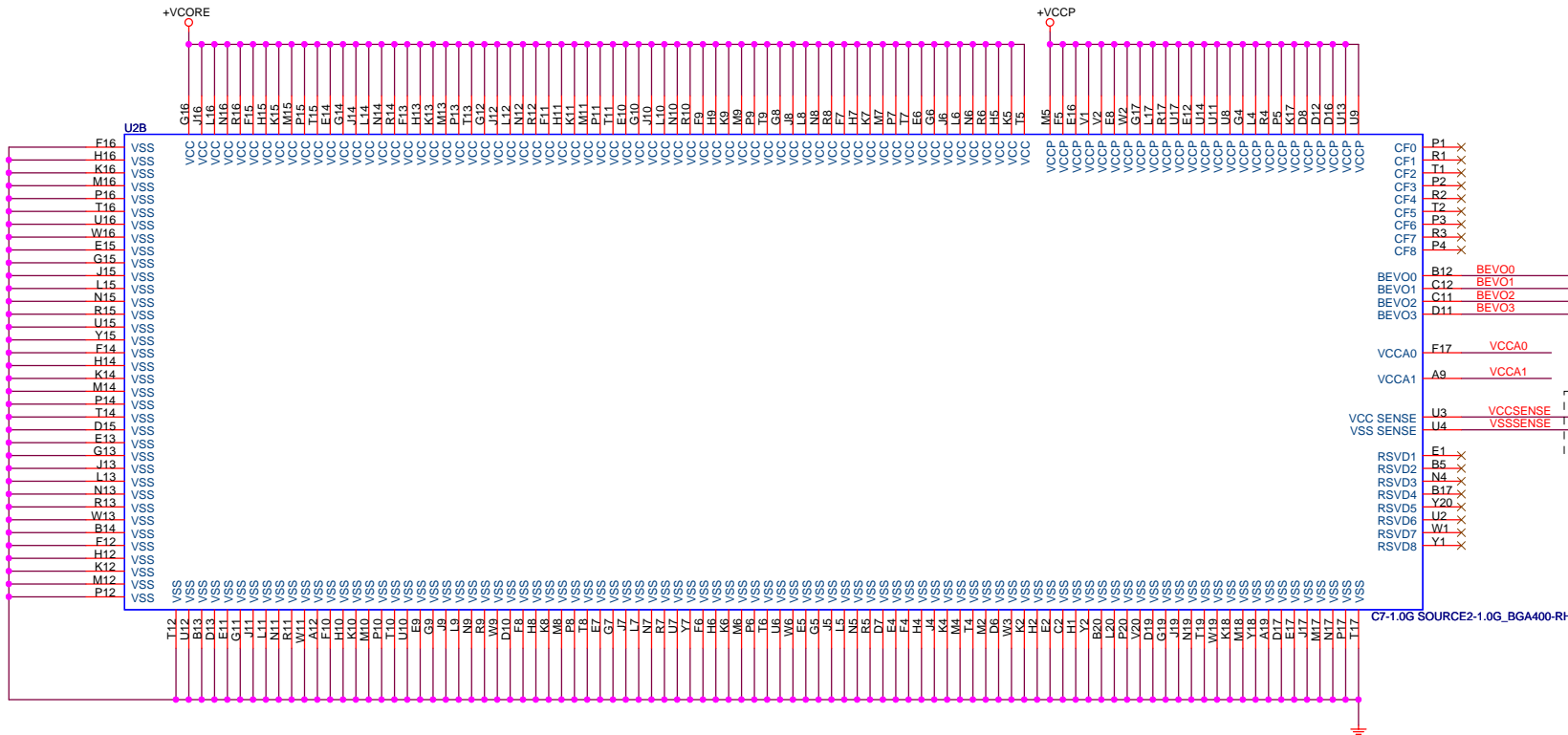




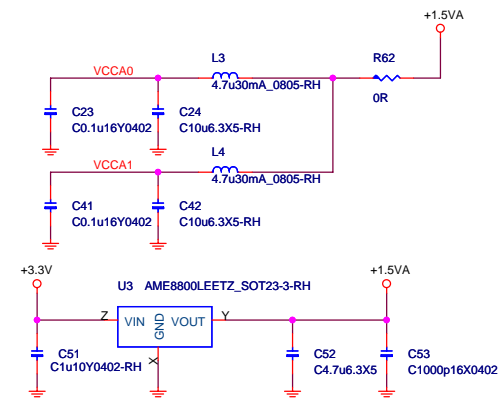
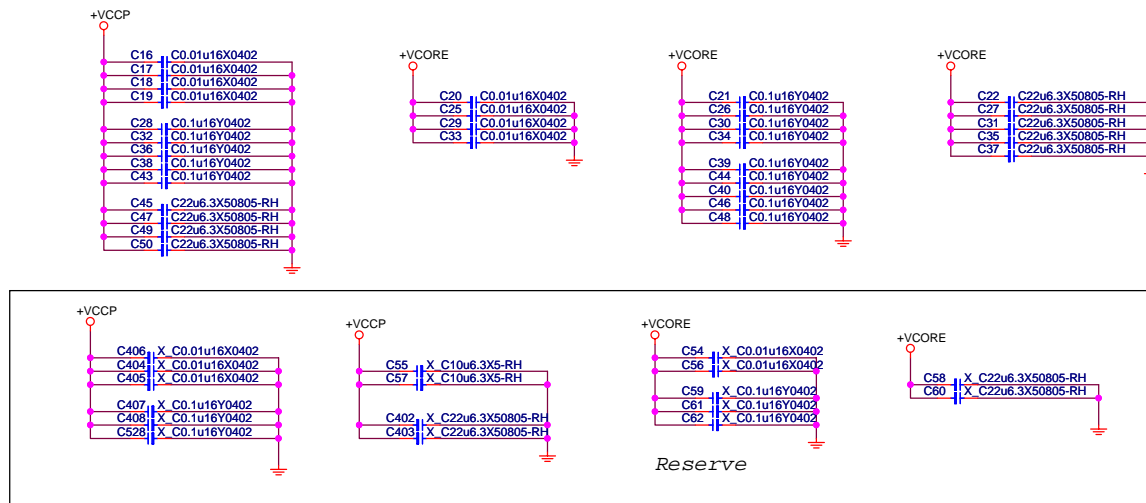
DEVICE

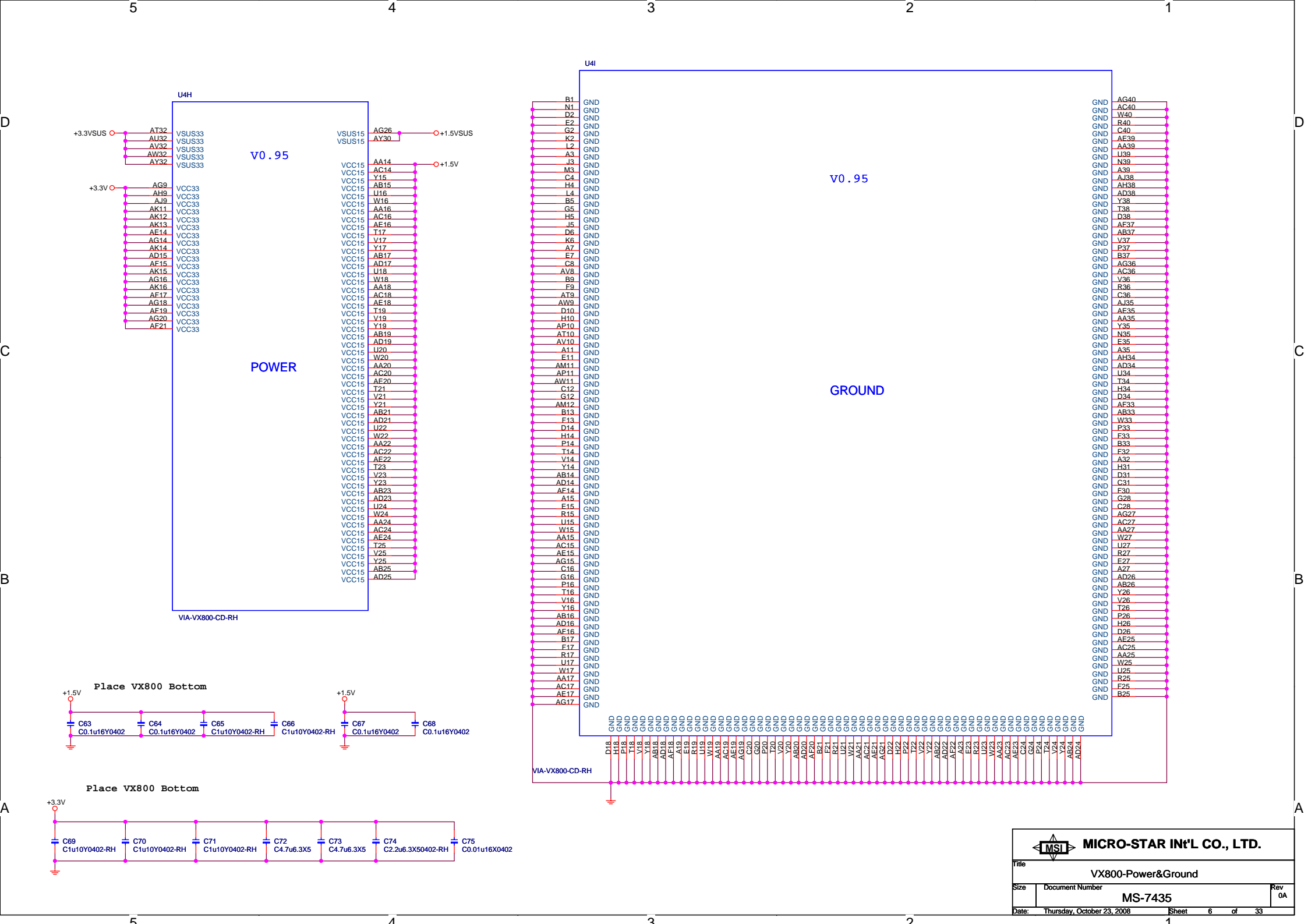
- CPU (1.116V / 17W)
- ALC888
- FAN,Hard Disk , PCIE X 4
- PS2 KB/MOUSE,USB
- IDE,2 X SATA , e-SATA
- VX800(0.74X2=1.5W)
DDR2 4A
- DDR2 (1.2A)
- VX800 (3.19W) Mini PCIE x 1 (1A)
- CPU (1.4W) , VX800 (0.028W)
- VX800 (0.03W)
- CPU (0.13A)
- VX800 (1.25W) VT1632 (0.09A)
- ALC888 (0.036A) e-SATA JM362 (0.05A)
- Clock Gen. (0.4A) PCIE x 4 (3A)
- Mini PCIE x 1 (1A)
- eSATA (0.35A / 0.63W)
- VX800 (175mW)
- LAN (55mA / 181.5mW)
- LAN (281mA / 421.5mW)
- LAN (102mA / 183.6mW)

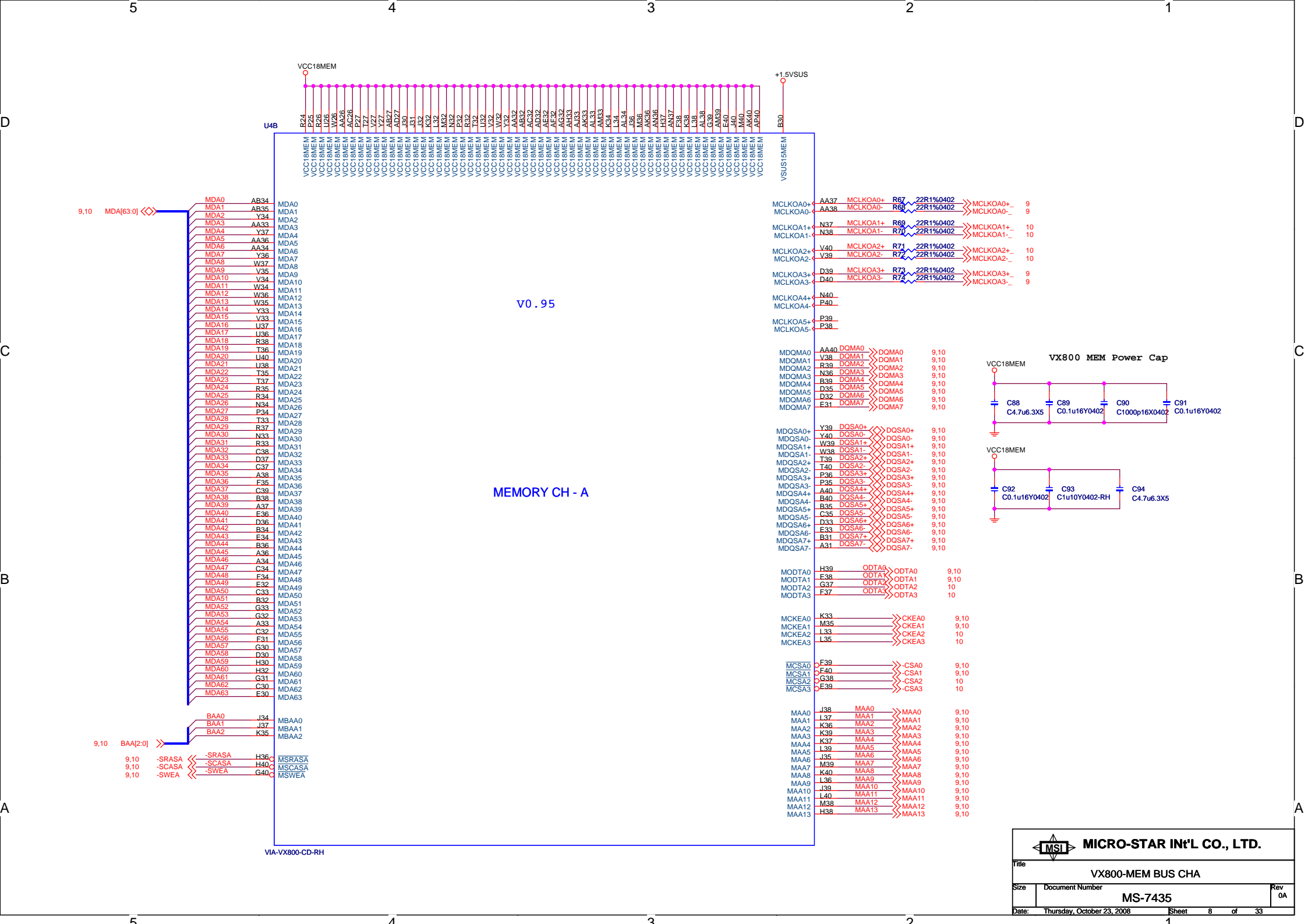


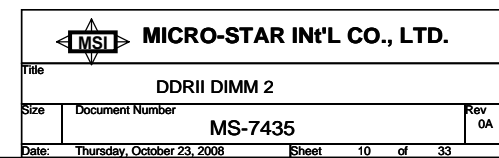


Follow AP430A

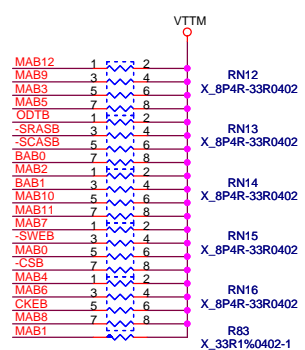
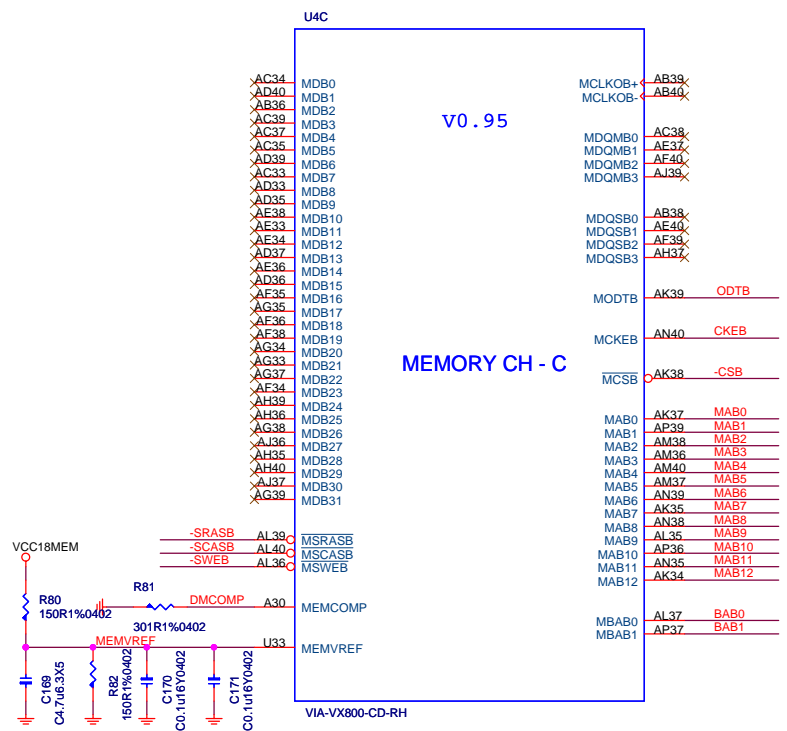




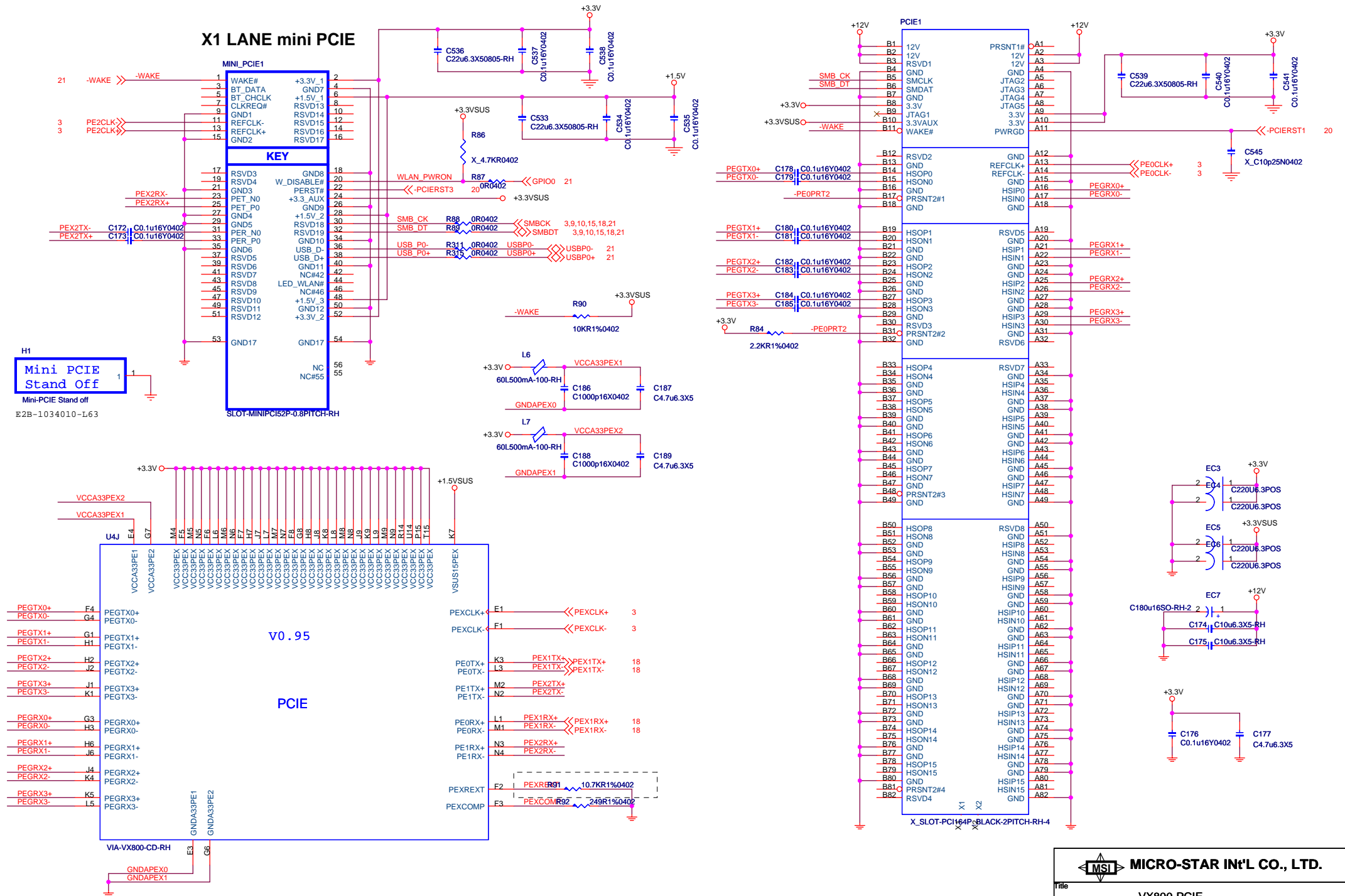


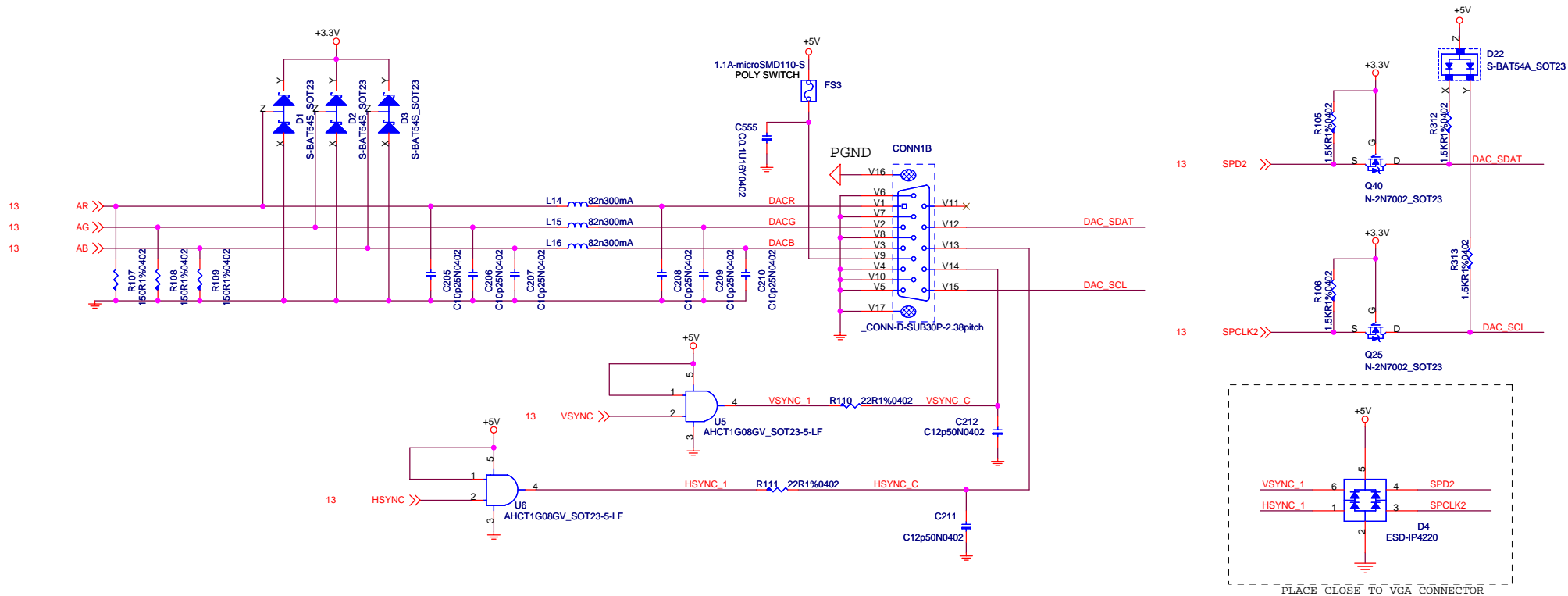


Schematic error , RN10 unmount ,RN11 mount ,
Remove R79,ODTA3 link to RN11---1007

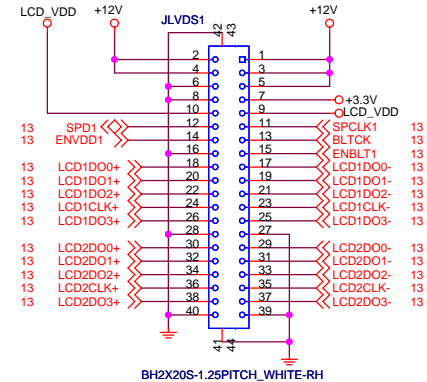
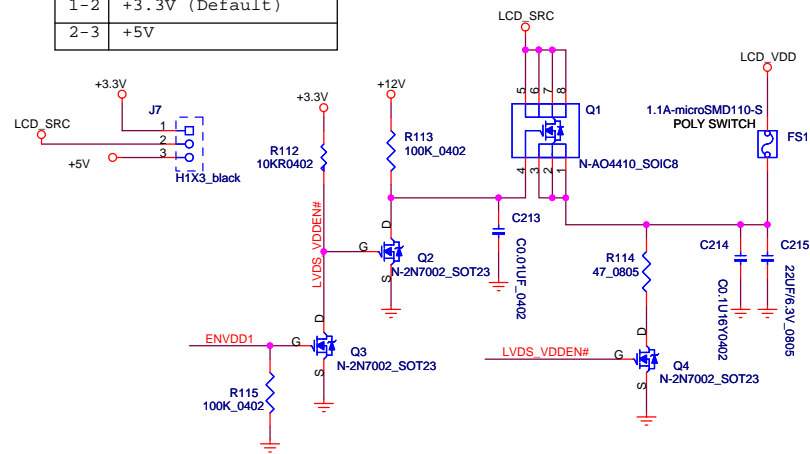


X1 LANE mini PCIE

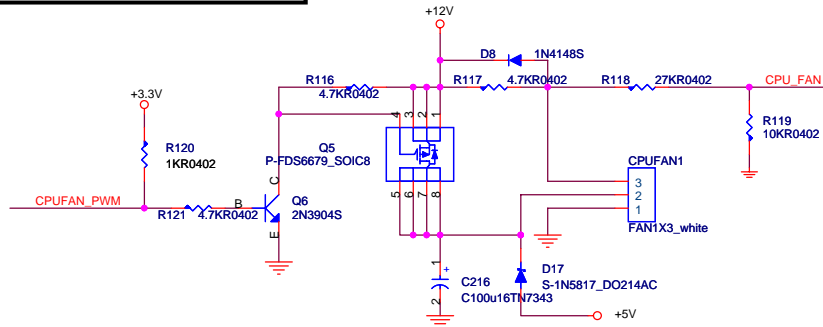




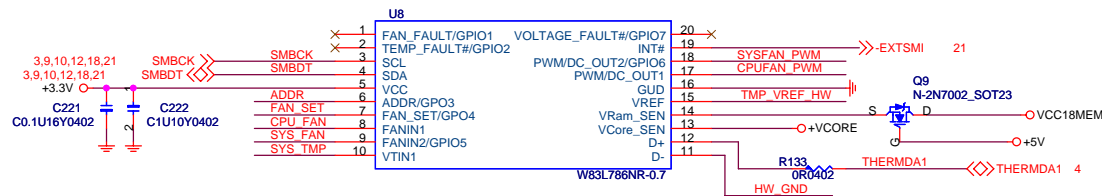
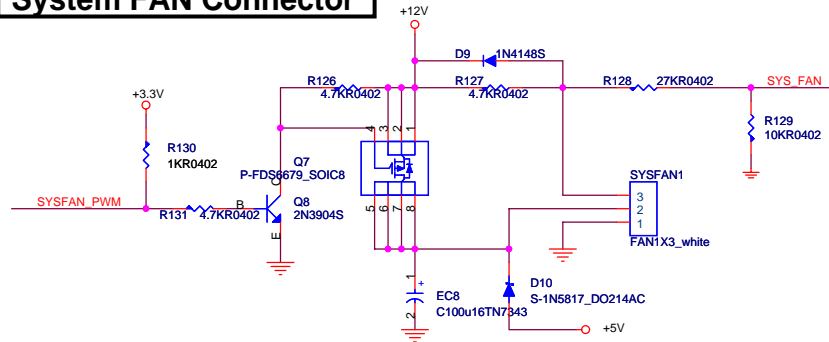
J7	LCD Power Select
1-2	+3.3V (Default)
2-3	+5V



CPU FAN Connector



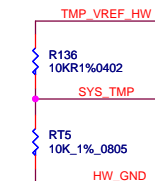
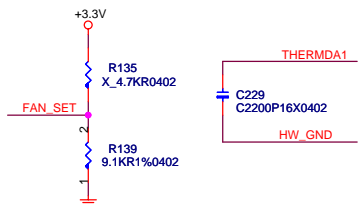
System FAN Connector



W83L786 Pin-17 & 18 are Open-Drain signals, they should be pulled up +3.3V

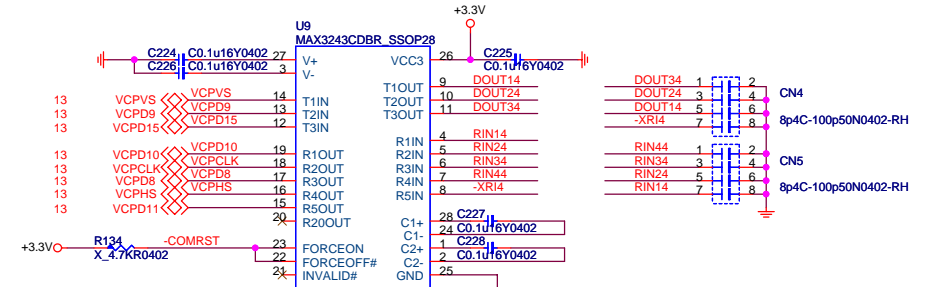
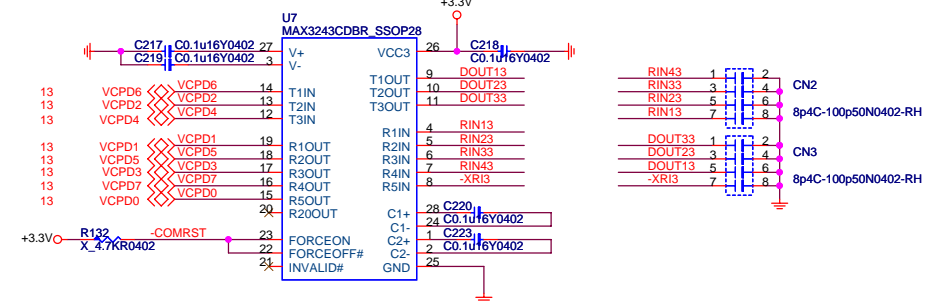
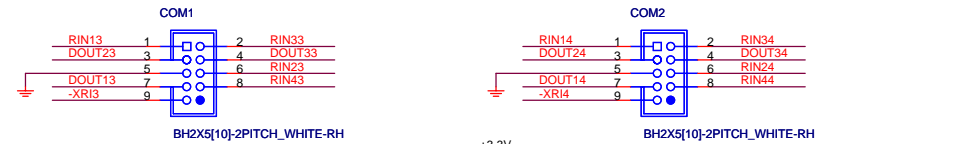
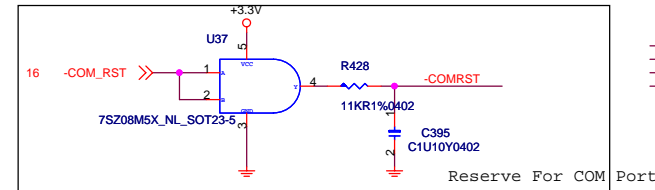
HI:Address = 0X5EH
LO:Address = 0X5CH
I2C Slave address select

NOTE: LOCATE CLOSE STATUS PANEL



VIA Suggest:The VCP port and COM port is multiple function and it is recognize which function is after Reset.
=>So, we recommend use "Reserve circuit for COM port" by default.
Unmount R132,R134
Mount U37,R428,C395,R332

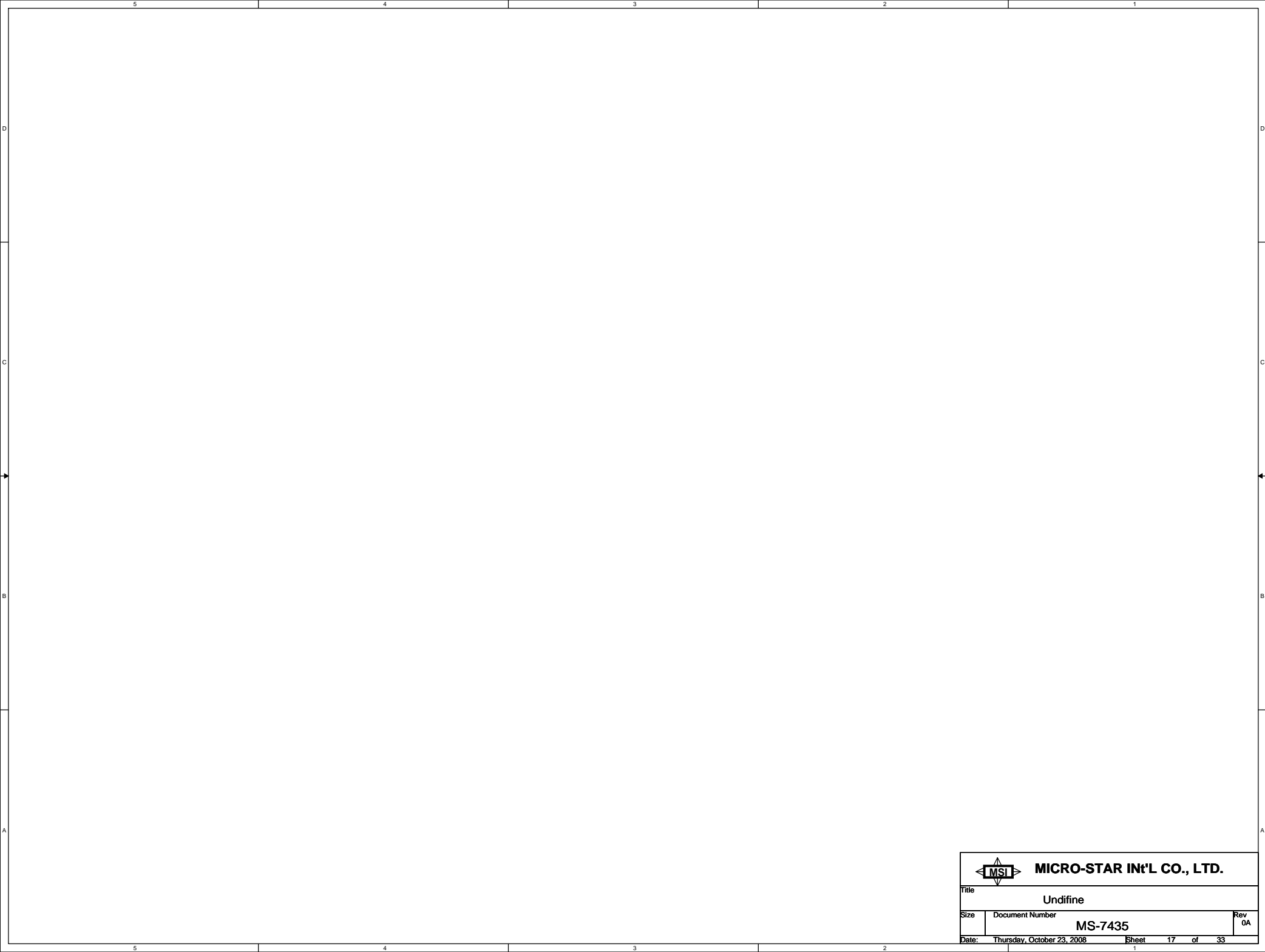
VCPD10	EXSR13[5]	CPUCK/MCK CLOCK Select
		* 0: from NB 1: from external
VCPD9	EXSR13[4]	PCI Signal test output enable
		* 0: Disable 1: Enable
VCPD7	EXSR13[0]	GFX CLOCK Select(VCK/LCDCK/ECK/TVCK)
		* 0: Refer internal 1: From external
VCPD6	EXSR12[6]	DVP0 port/Capture port select
		* 0: Capture port 1: DVP0 port
		★stand for default setting




COM port

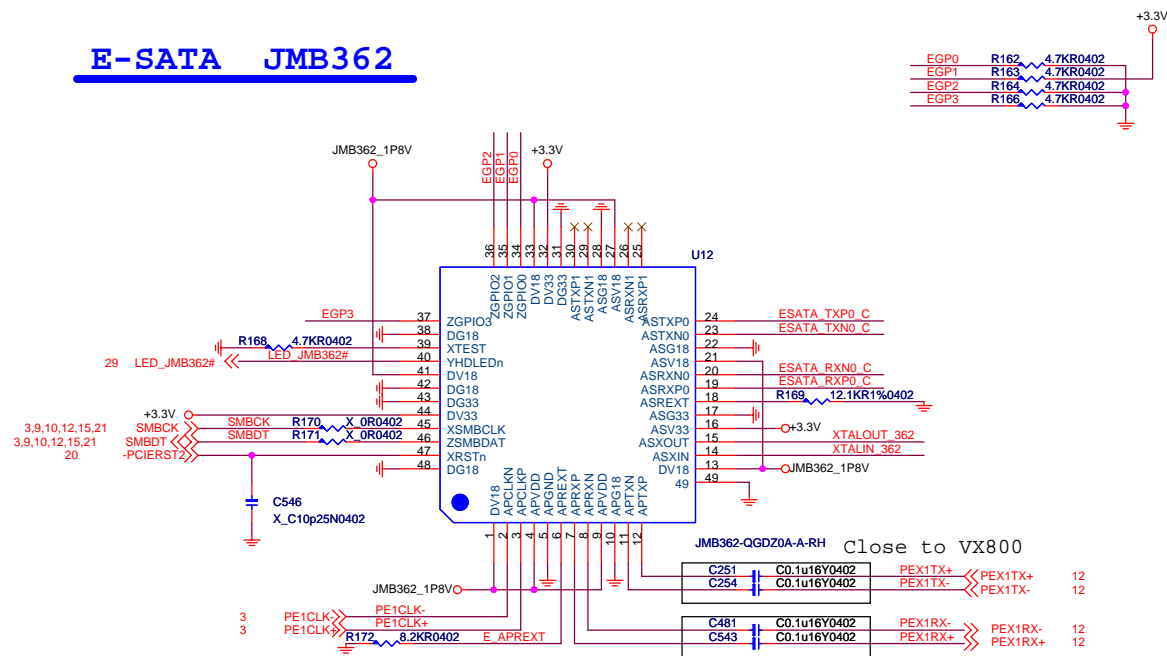
MICRO-STAR INT'L CO., LTD.			
Title			
COM PORT&HWM			
Size	Document Number	Rev	
	MS-7435	0A	
Date	Thursday, October 23, 2008	Sheet	15 of 33

9/8 VIA suggest : -SERR & -DEVSEL need pull up 2.7K ohm to +5V



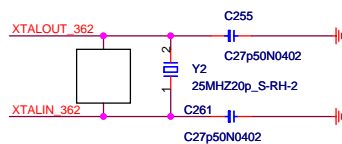
 MICRO-STAR INT'L CO., LTD.		
Title Undifine		
Size	Document Number MS-7435	Rev 0A
Date: Thursday, October 23, 2008		
Sheet 17 of 33		

E-SATA JMB362

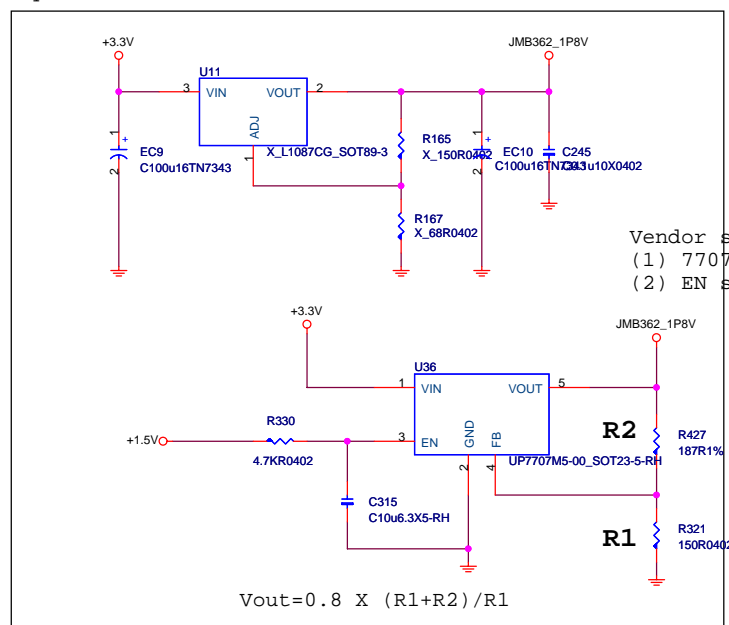
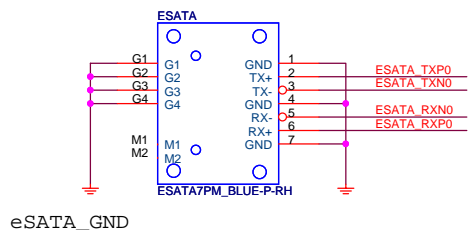
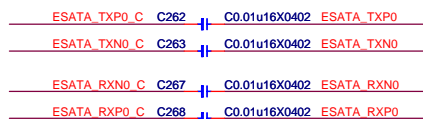


Close to U12

PS: The AC Cap should be place at Transition side of Device if your device is onboard.

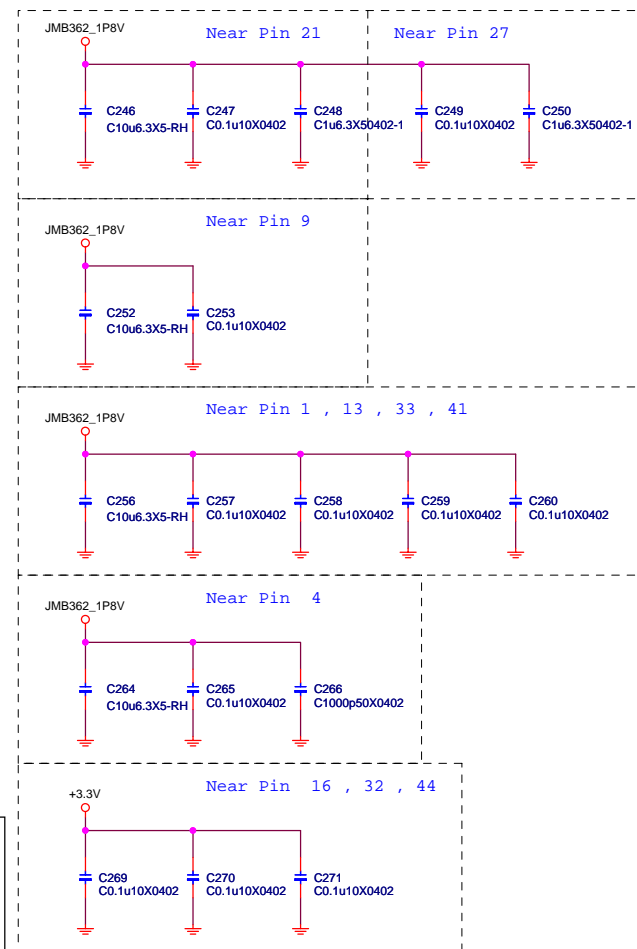


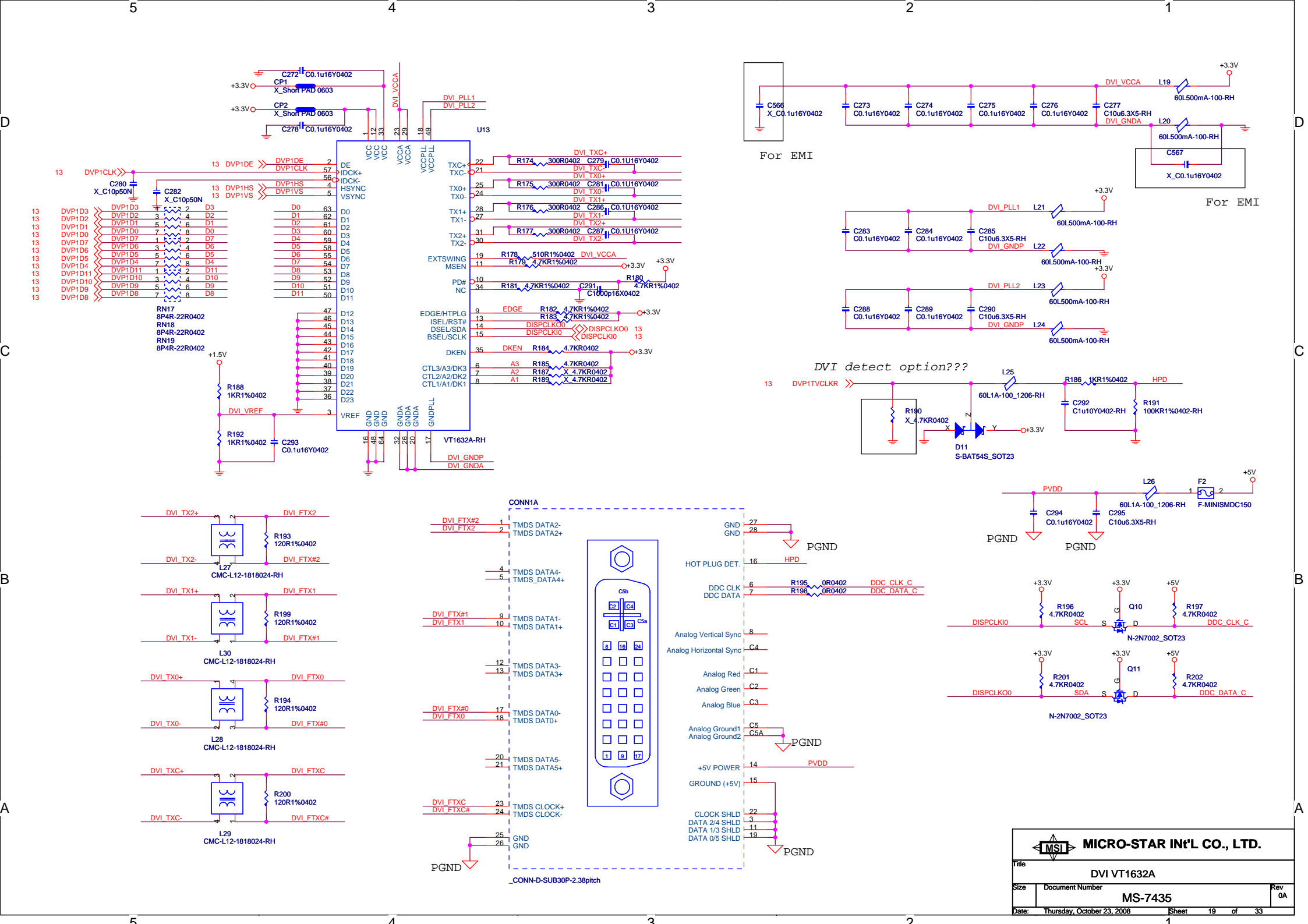
Remove R173

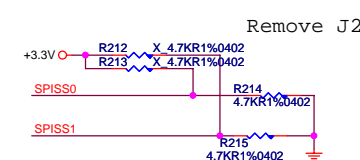
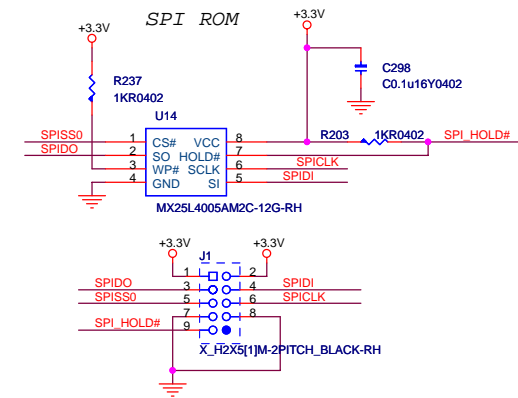
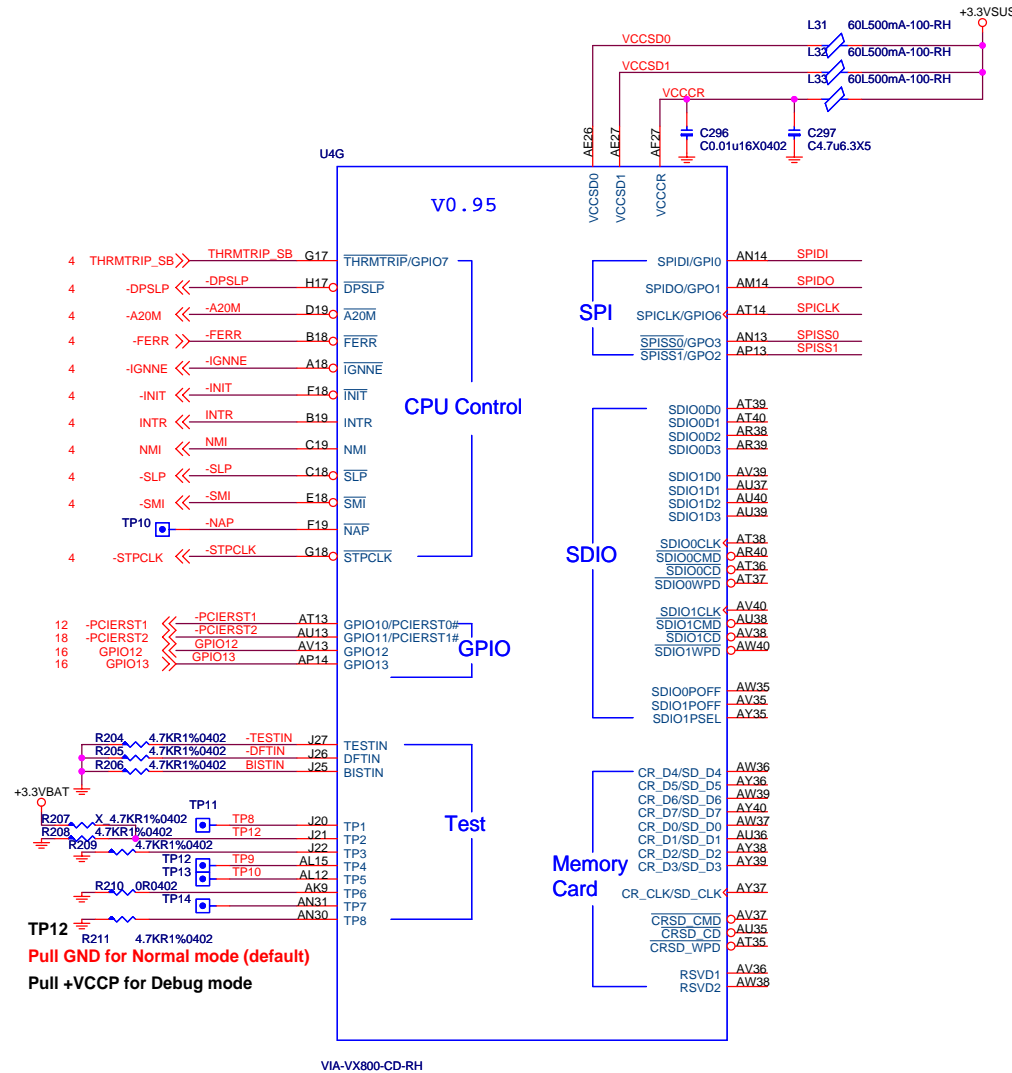


Vendor suggest, reserve:

- (1) 7707 and LDO co-layout
- (2) EN signal of 7707 is active after 40ms when 3.3V power ok

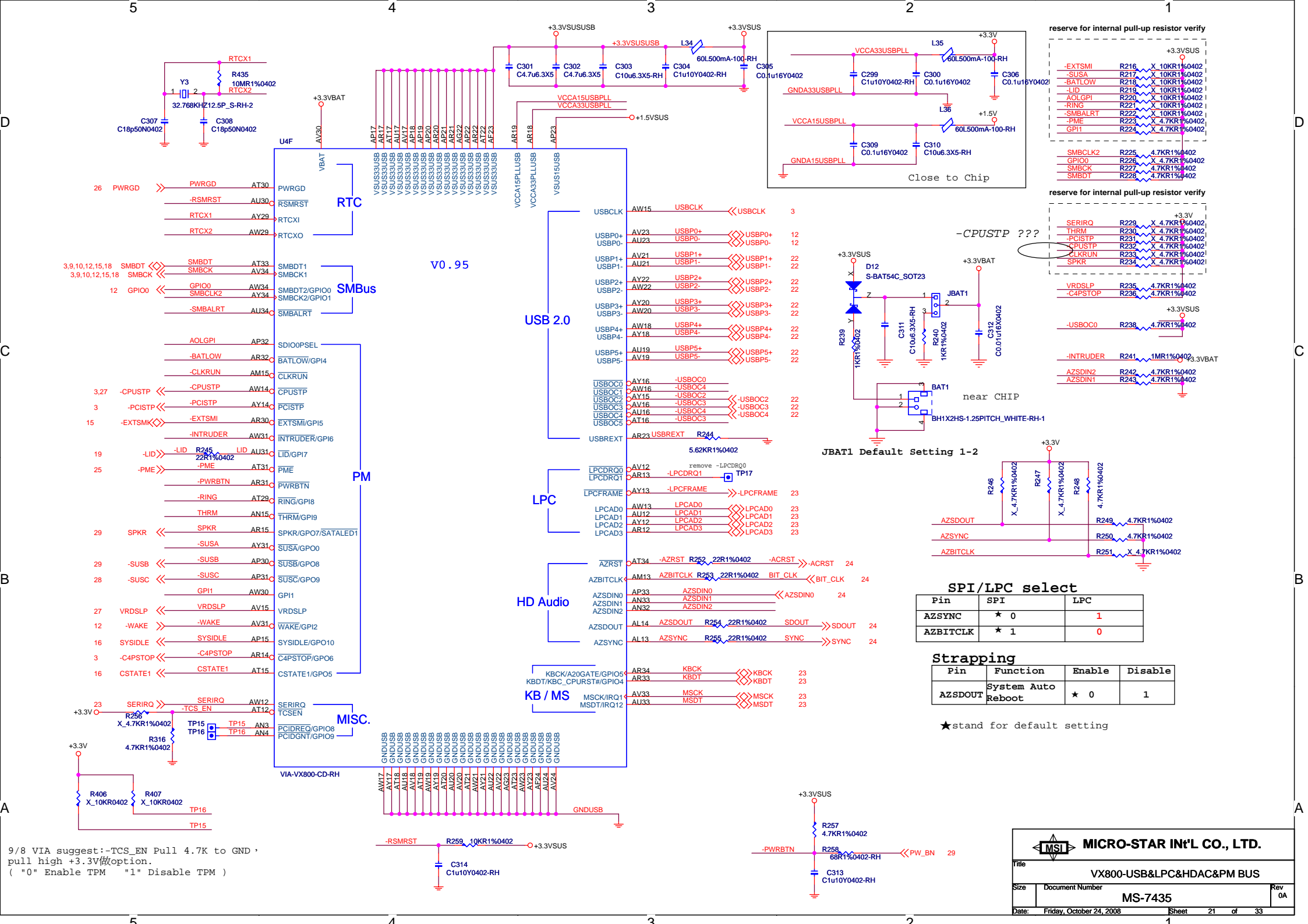


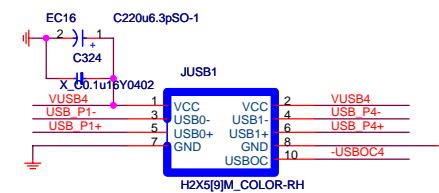
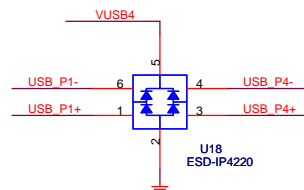
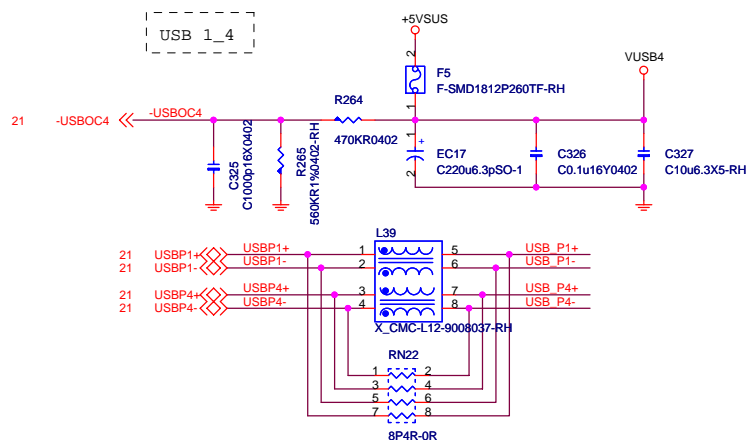
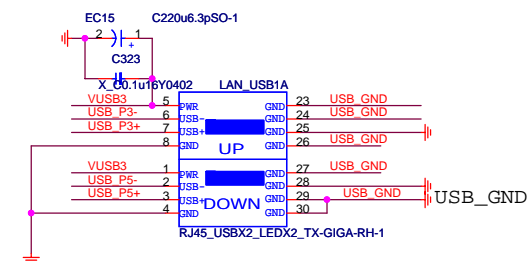
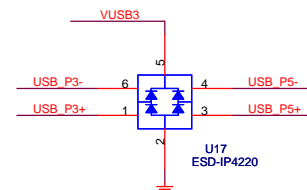
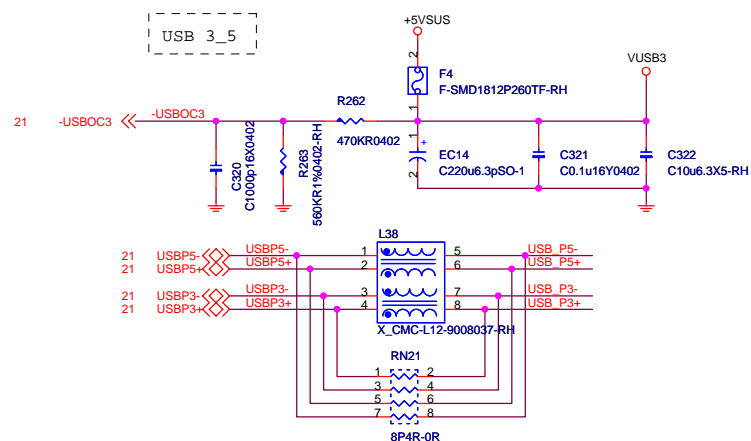
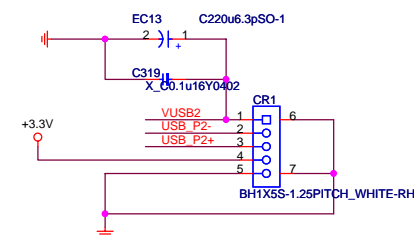
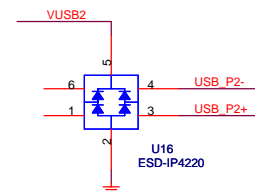
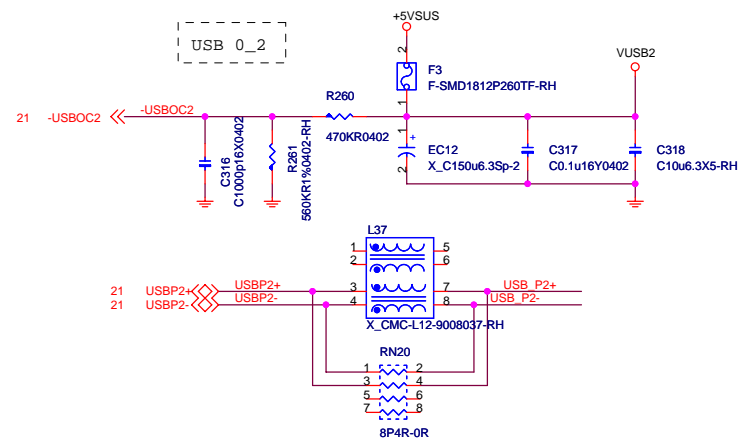




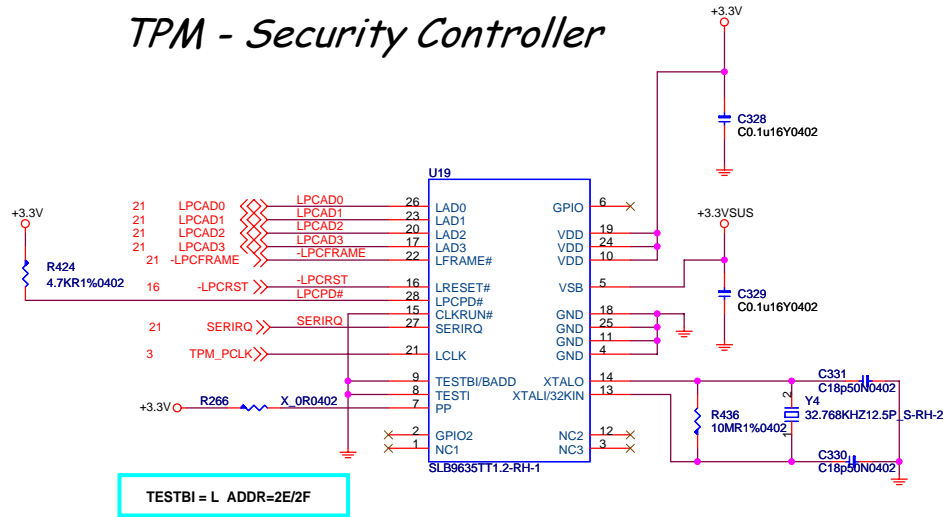
Pin	SPISS1	SPISS0 (J2)	Function
Select	★ Must low	★ Short	IDE
		Open	NFC

★stand for default setting

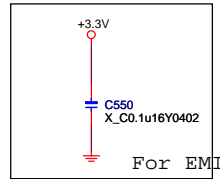




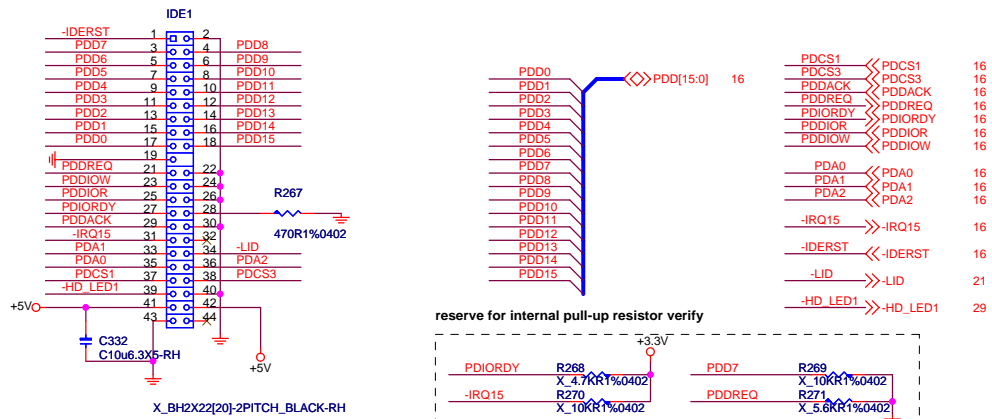
TPM - Security Controller



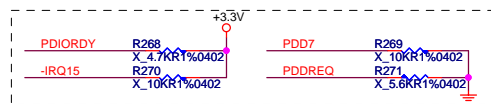
TESTBI = L ADDR=2E/2F



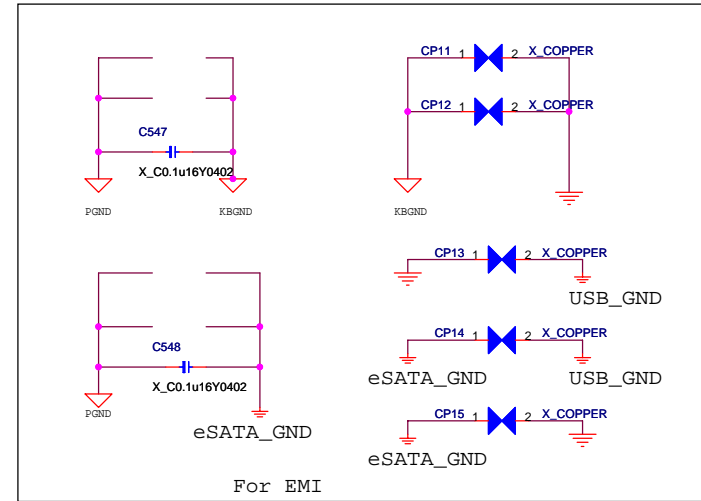
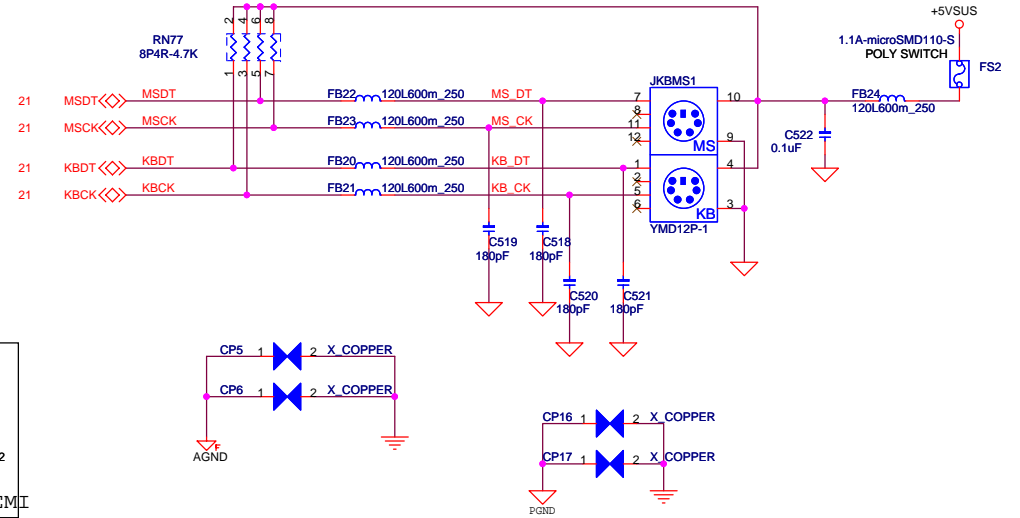
PRIMARY



reserve for internal pull-up resistor verify



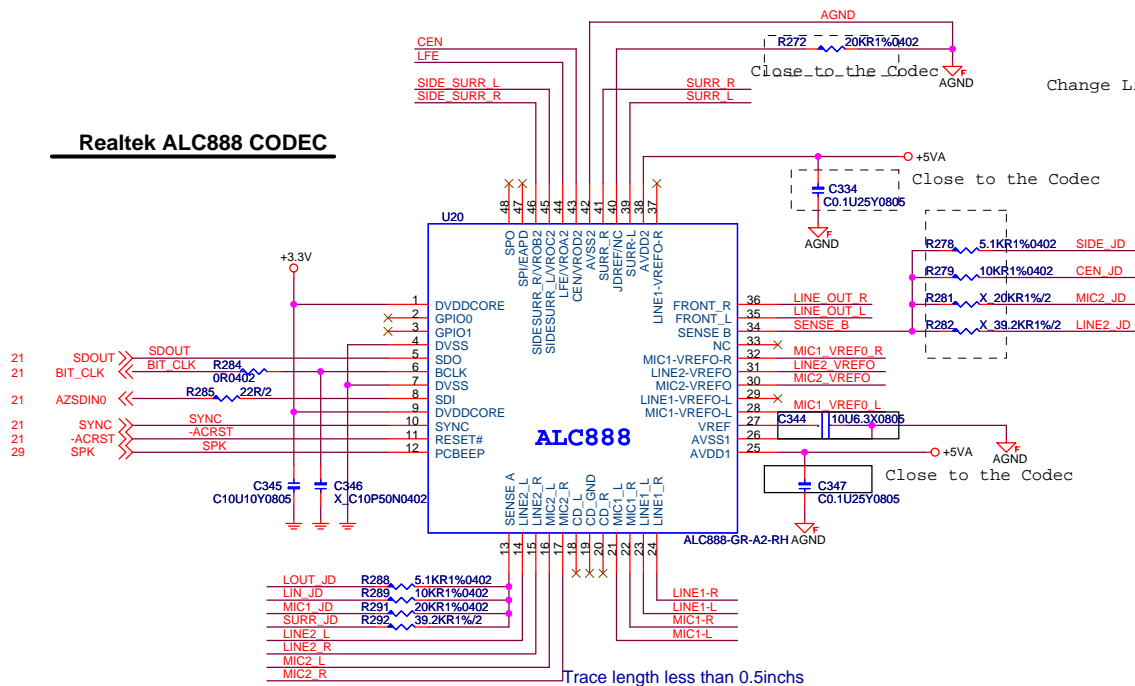
PS2 KEYBOARD & MOUSE CONNECTOR



MICRO-STAR INT'L CO., LTD.

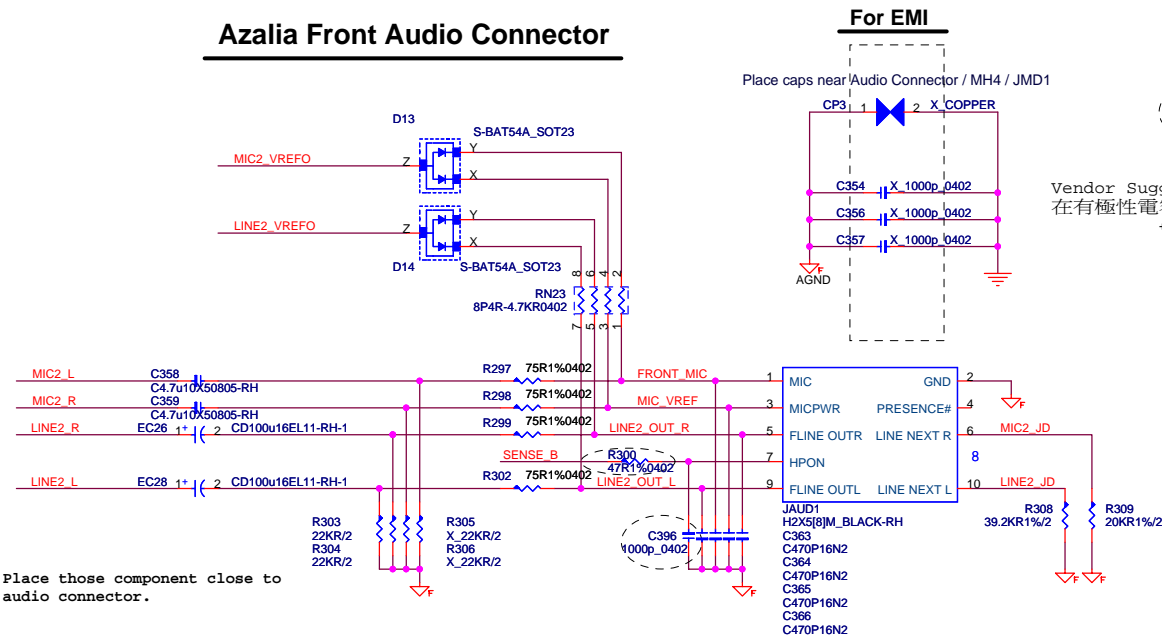
Title		TPM&PATA
Size	Document Number	MS-7435
Date	Thursday, October 23, 2008	Sheet 23 of 33

Realtek ALC888 CODEC



Note: GND連接點擺放位置避開Power走線以及Noise干擾

Azalia Front Audio Connector



Place those component close to audio connector.

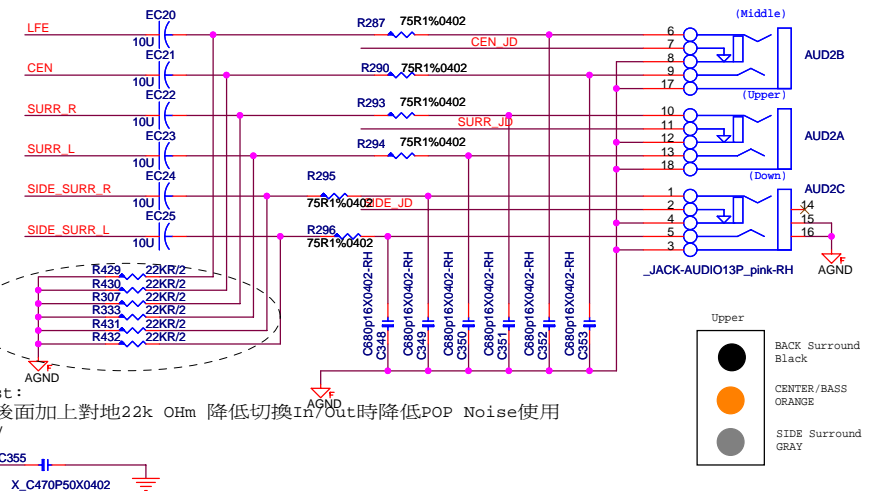
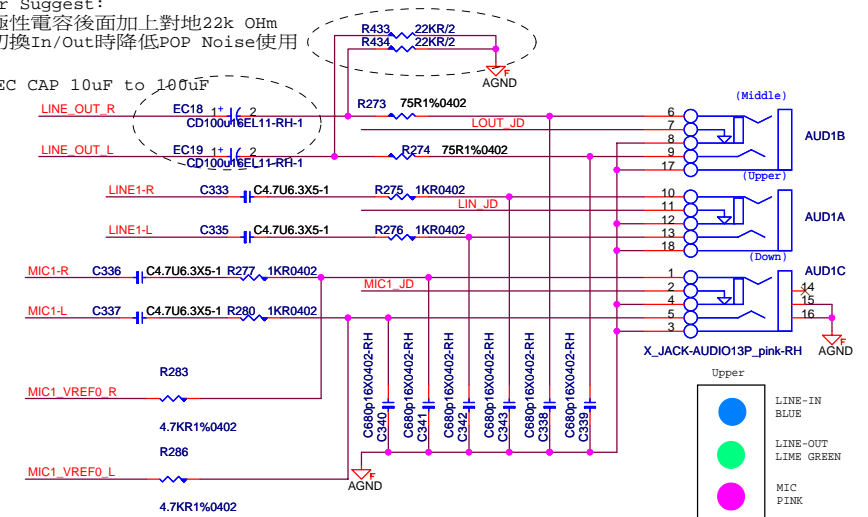
Vendor suggest:
Change R300 to 470hm, and near the front panel
Change to 1000pF, and near the front panel

PHONE JACKER (HDA JACK)

Vendor Suggest:

在有極性電容後面加上對地22k OHm
降低切換In/Out時降低POP Noise使

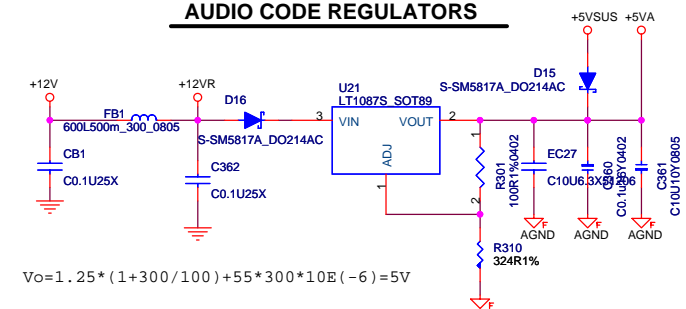
Change Line Out EC CAP 10uF to 100uF



Vendor Suggest :

在有極性電容後面加上對地22k OHm 降低切換In/Out時降低POP Noise使用

AUDIO CODE REGULATORS



$$V_0 = 1.25 * (1 + 300/100) + 55 * 300 * 10E(-6) = 5V$$

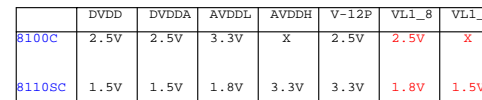


➤ **MICRO-STAR INT'L CO., LTD.**

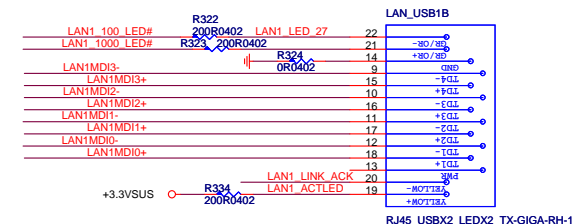
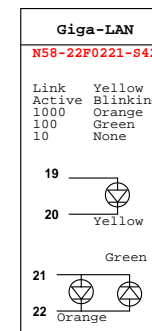
Title HD AUDIO CODEC ALC888-GR

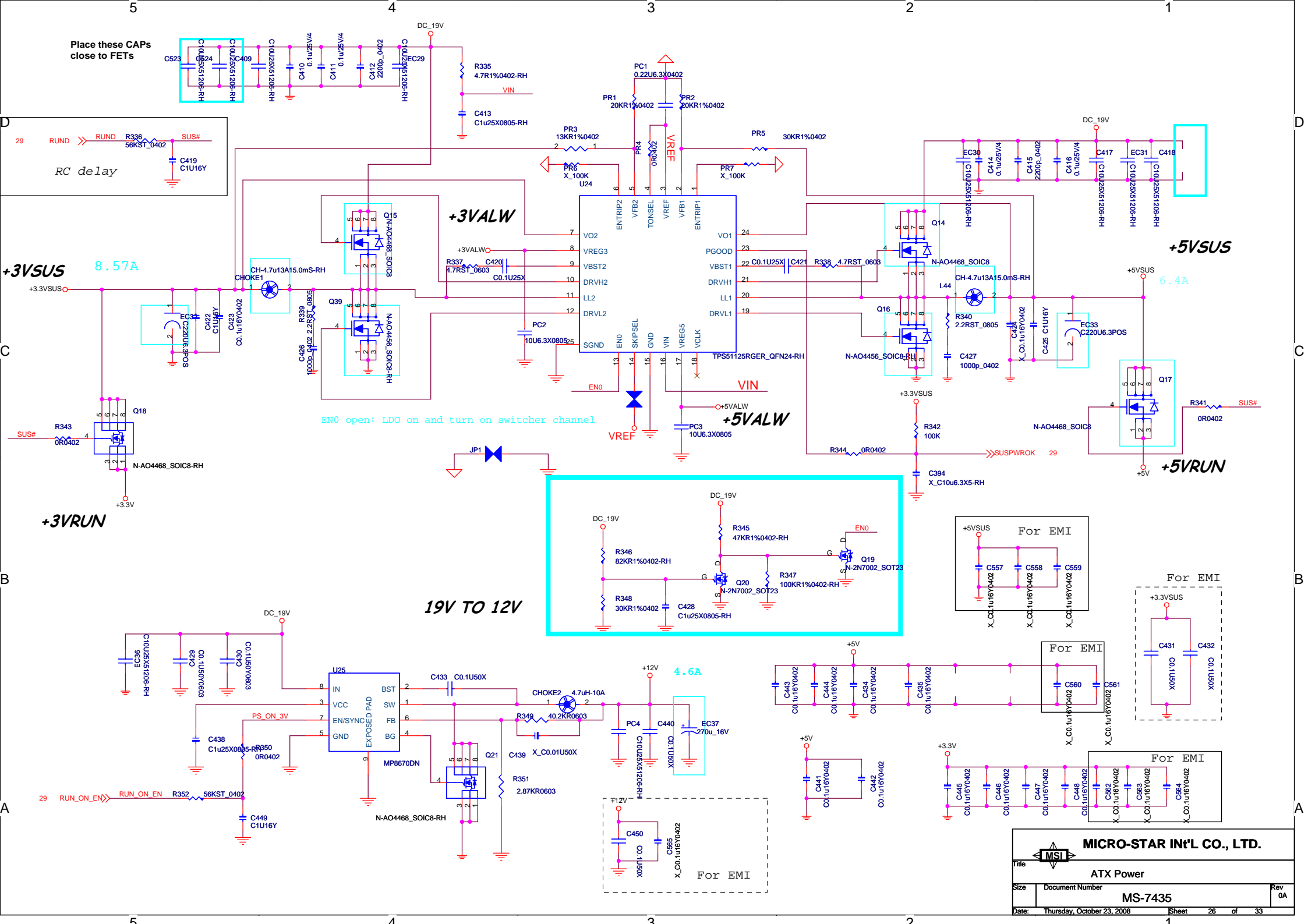
Size	Document Number
	MS-7435

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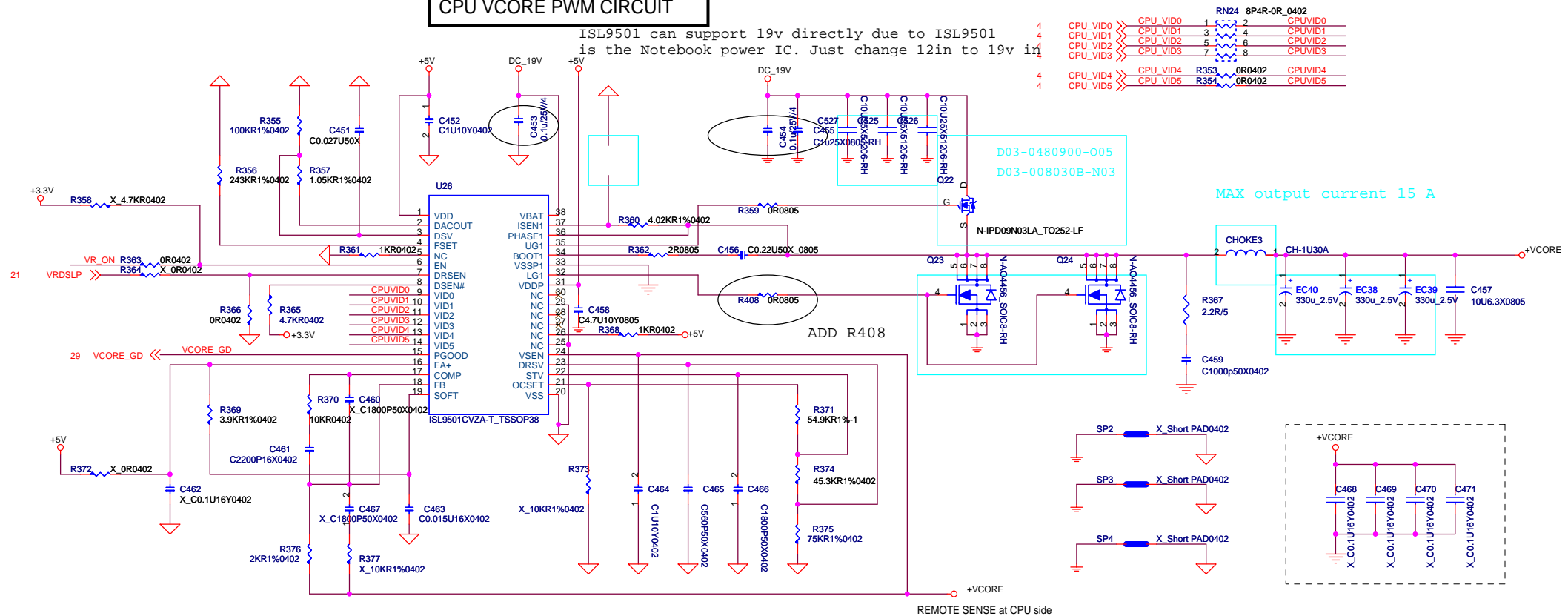
LAN1 CONNECTOR





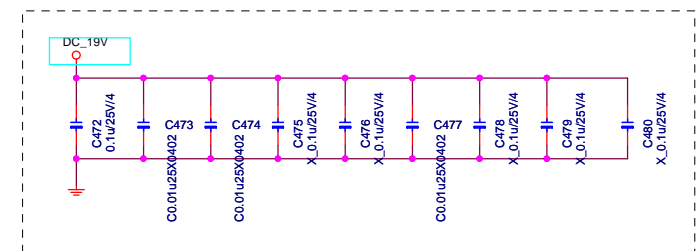
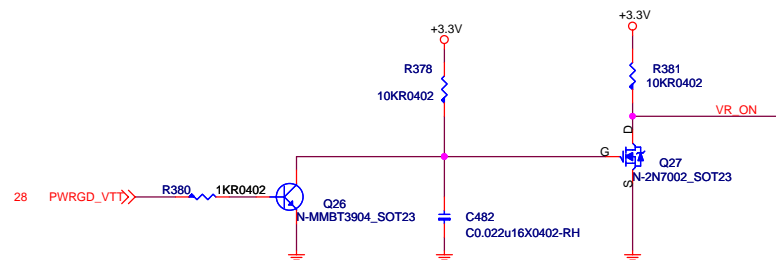
CPU VCORE PWM CIRCUIT

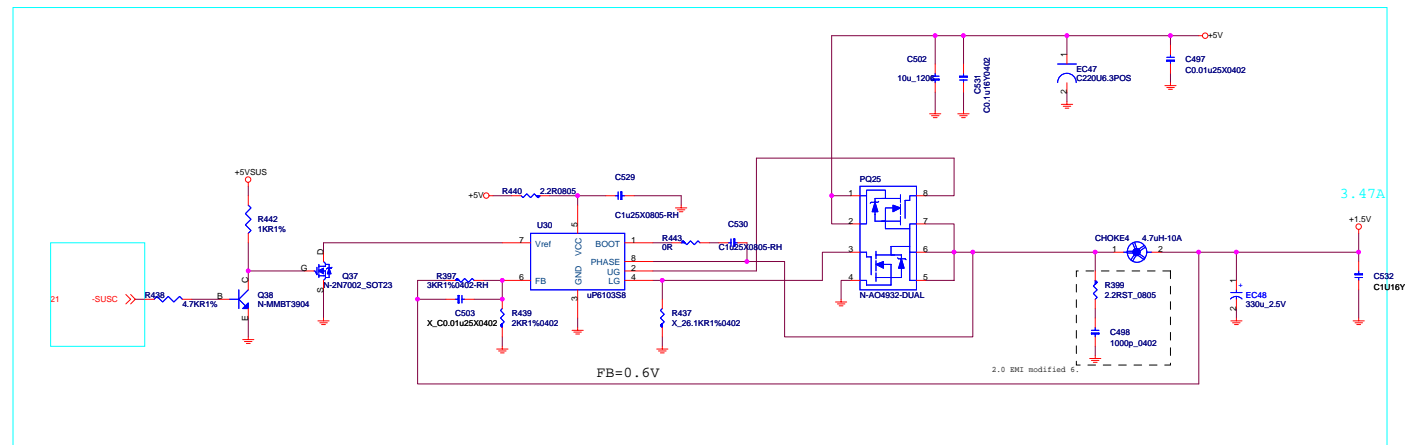
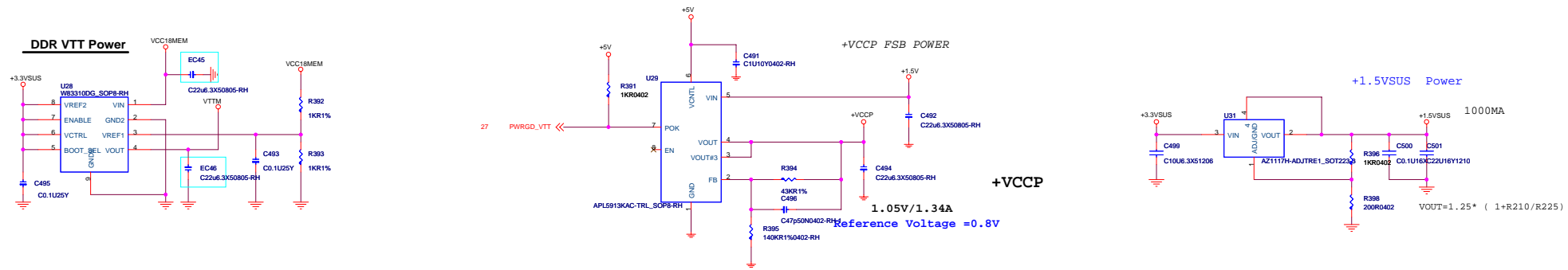
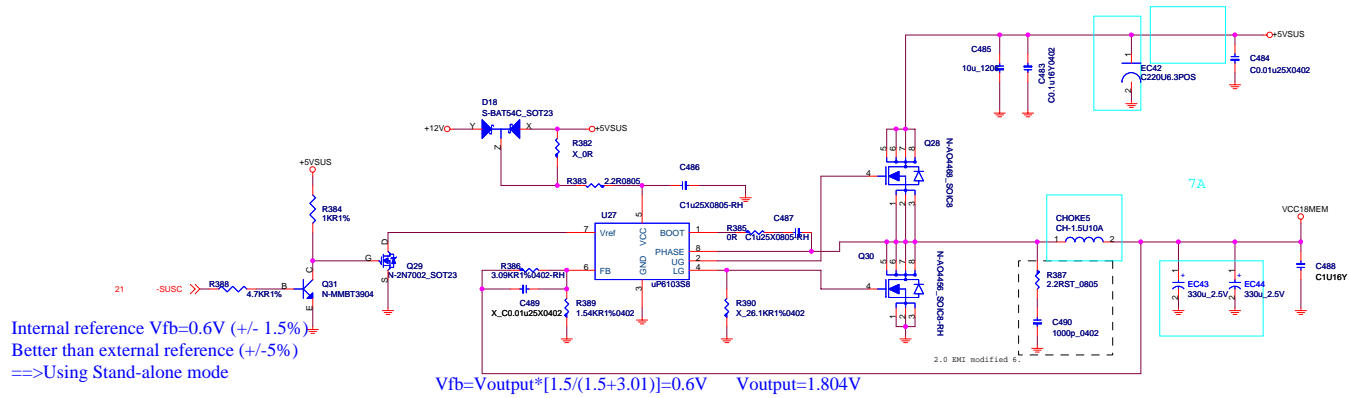
ISL9501 can support 19v directly due to ISL9501
is the Notebook power IC. Just change 12in to 19v in

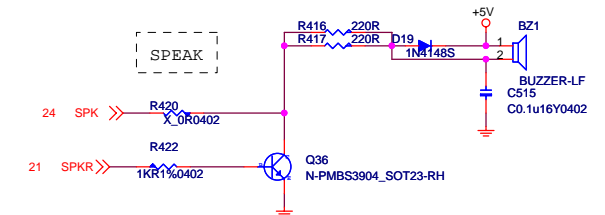
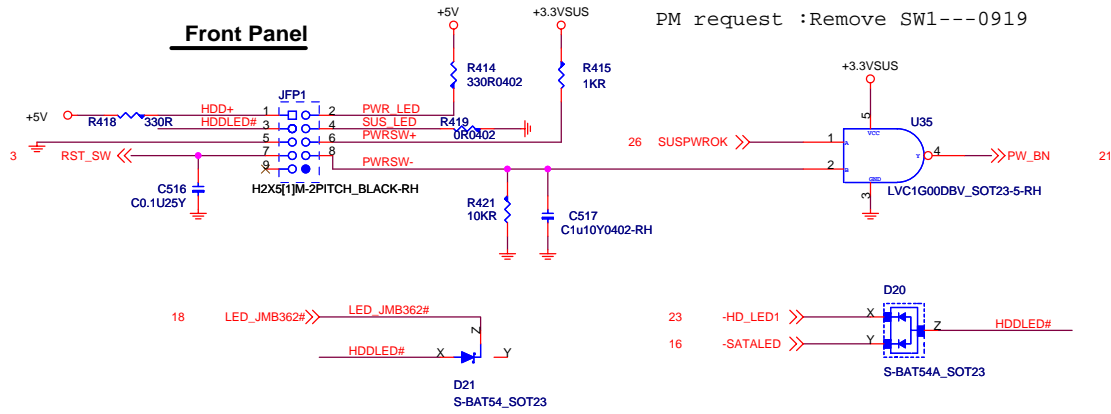
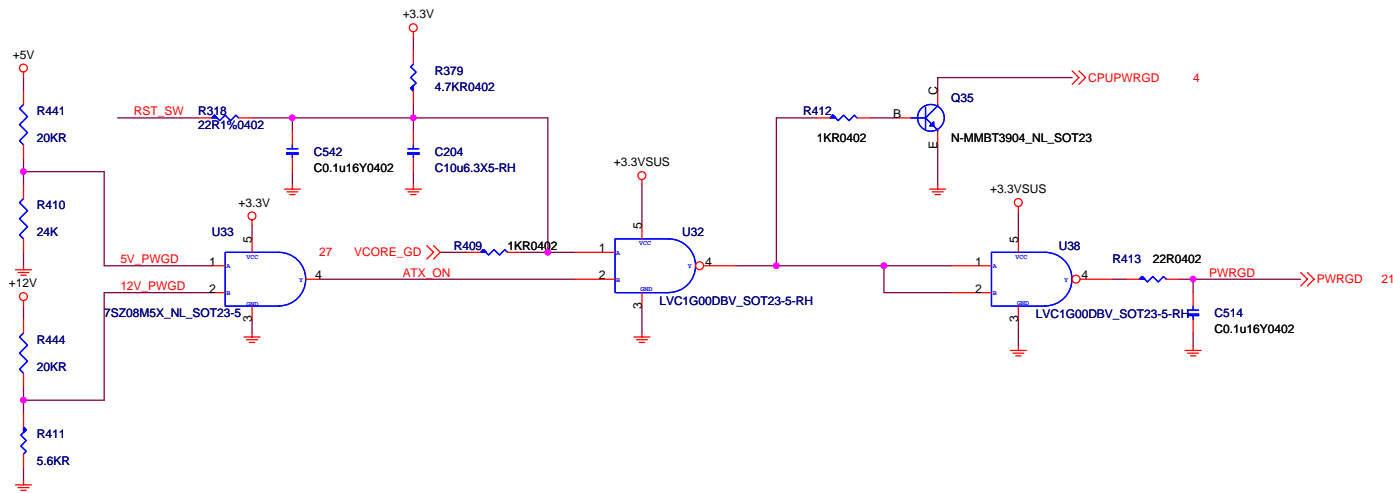
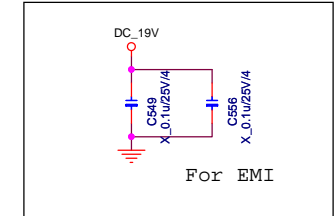
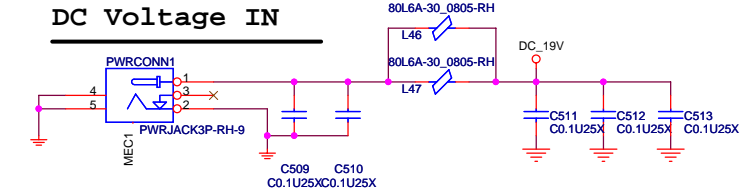
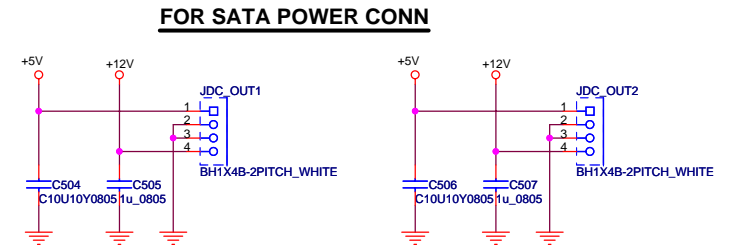
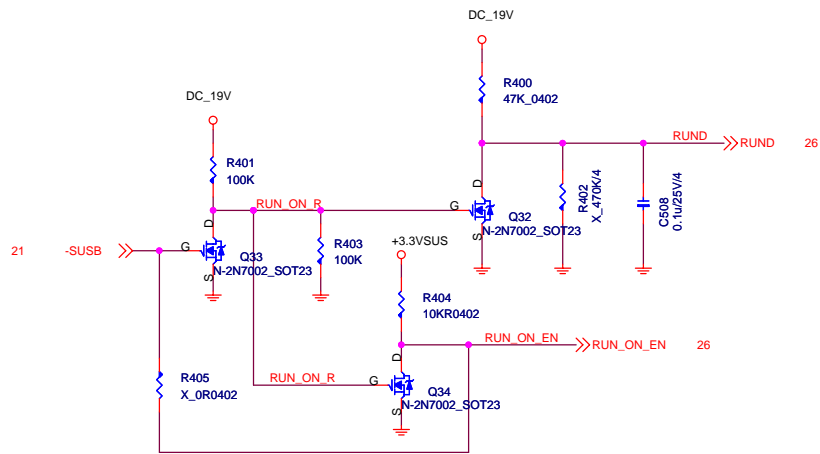


Remove:CLK_EN to P3,-CPUSTP to P3&21,VCCSENSE to P5,-PSI to P4

VIA suggest : If your CPU PWM is not CLK enable function pin.
=>We recommend the CLK enable pin connect 10k ohm to +3.3V directly.
Unmount Q25 and C481,R379







Clock Generator (ICS9UM700)				
PIN NO	PIN NAME	CONNECT TO		
53	CPUT_L0	CPU_CLK	=>	CPU BCLK
52	CPUC_L0	-CPU_CLK	=>	CPU BCLK#
49	CPUT_L1F	HCLK+	=>	NB HCLK+
48	CPUC_L1F	HCLK-	=>	NB HCLK-
45	PCIEXT_L0/CPU_ITPT	PE0CLK+	=>	PCIE X4 LANE
44	PCIEXC_L0/CPU_ITPC	PE0CLK-	=>	PCIE X4 LANE
43	PCIEXT_L1	PEXCLK+	=>	NB PEXCLK+
42	PCIEXC_L1	PEXCLK-	=>	NB PEXCLK-
39	PCIEXT_L2	PE1CLK+	=>	PCIE X1 LANE
38	PCIEXC_L2	PE1CLK-	=>	PCIE X1 LANE
37	PCIEXT_L3	PE2CLK+	=>	PCIE X1 LANE
36	PCIEXC_L3	PE2CLK-	=>	PCIE X1 LANE
6	PCICLK_F0_2X	PCICLK_VX800	=>	SB PCICLK
7	SEL_ITP/PCICLK1_2X	PCI_CLK1	=>	PCI LAN
8	PCICLK2_2X			
11	PCICLK3			
12	PCICLK4	LPCROM	=>	LPCROM
13	PCICLK5			
17	FSLC/3V66_0F	GCLK(FSLC)	=>	** FSLC ** / NB GCLK
1	FSLA/REF0	XIN(FSLA)	=>	** FSLA ** / GRAPHIC MISC.
29	48MHz_0	LPCSTO_OSC	=>	LPC SUPER IO CLKIN
30	48MHz_1	USBCLK	=>	SB USBCLK
26	DISPCLKOUT	DISPCKO	=>	NB DISPCLKI1
25	DISPCLKIN	DISPCKI	=>	NB DISPCLKO1
22	FSLB/25MHz_LAN	25MHZ_LAN(FSLB)	=>	** FSLB ** / PCI LAN
21	25MHz_SATA	CS25MHZ	=>	SATA PCIE X4 LANE

PCI Device ID number

PCI Device	IDSEL	Device#	INT_A#	REQ#	GNT#
LAN VT6122	AD22	0Bh	INT_D#	-REQ3	-GNT3

J7 LCD Power Select
1-2 Short :+3.3V
2-3 Short :+5V

	DATA	CLOCK
JLVDS	SPD1	SPCLK1
DVI	DISPCKO0	DISPCKIO

★stand for default setting

★ FSB800

FSB400

3	2	1		
FSLA	FSLC	FSLB	CPU	PCI
0	0	0	266.66	33
1	0	0	133.33	33
0	0	1	200	33
1	0	1	166.66	33
0	1	0	333.33	33
OFF	OFF	0	100	33
0	1	1	400	33
1	1	1	RESERVED	

	ON	OFF
4	★ Pin45,44 Set PCI-E CLK Pair	Pin45,44 Set ITP CLK Pair

J2

Pin	SPISS1	SPISS0 (J2)	Function
Select	★ Must low	★ Short	IDE
		Open	NFC

SPI/LPC select

Pin	SPI	LPC
AZSYNC	★ 0	1
AZBITCLK	★ 1	0

Strapping

Pin	Function	Enable	Disable
AZSDOUT	System Auto Reboot	★ 0	1

FSB Freq Strapping


Pin	Select	FSB Freq.
GPIO12/ CSTATE1 (2/ 1)	00	100Mhz
	01	Reserved
	10	200Mhz
	★ 11	Auto Mode

Strapping signals

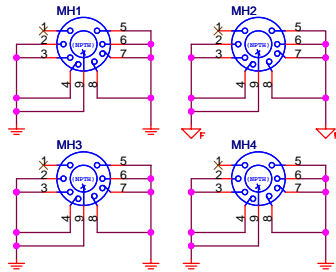
Pin	Function	0	1
PDA1	Dual/Single	★ Single	Dual
PDA0		★ Always low	
GPIO13	GTL pull up	★ Enable	Disable
SYSIDLE	IOQ depth	★ 12	1
PDA2	PLL_OK Selection	★ PLL	Logic counter

VCPD10	EXSR13[5]	CPUCK/MCK CLOCK Select ★ 0: from NB 1: from external
VCPD9	EXSR13[4]	PCI Signal test output enable ★ 0: Disable 1: Enable
VCPD7	EXSR13[0]	GFX CLOCK Select(VCK/LCDCK/ECK/TVCK) ★ 0: Refer internal 1: From external
VCPD6	EXSR12[6]	DVP0 port/Capture port select ★ 0: Capture port 1: DVP0 port

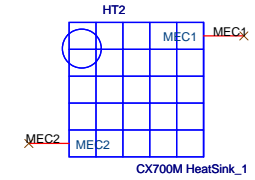
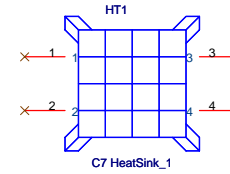
★stand for default setting

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Size	Document Number MS-7435	Rev 0A
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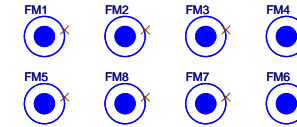
Mounting Holes



Auto-BOM Manual Parts



Optics Orientation Holes

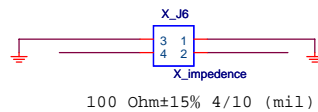
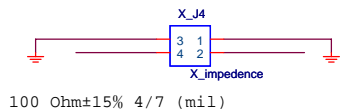
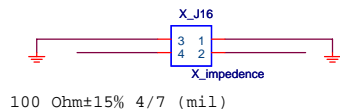
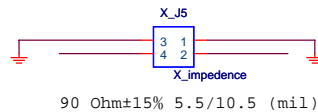
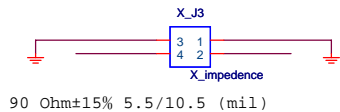
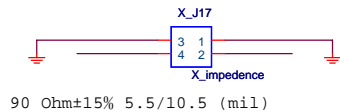
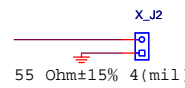
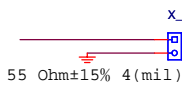
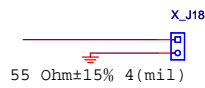
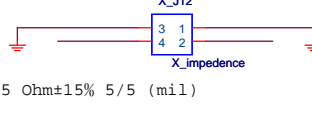
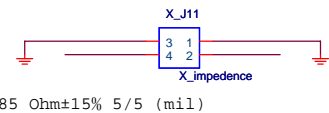
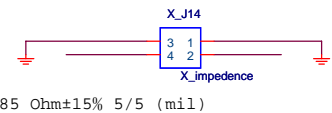
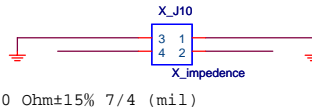
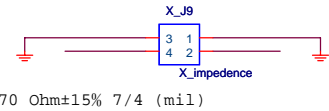
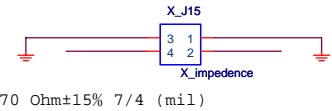
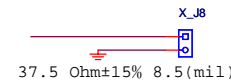
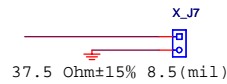
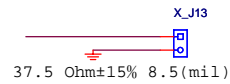


Simulation

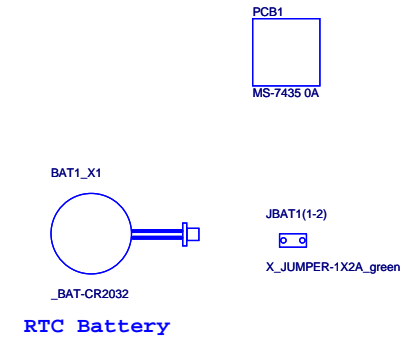
Bottom Layer

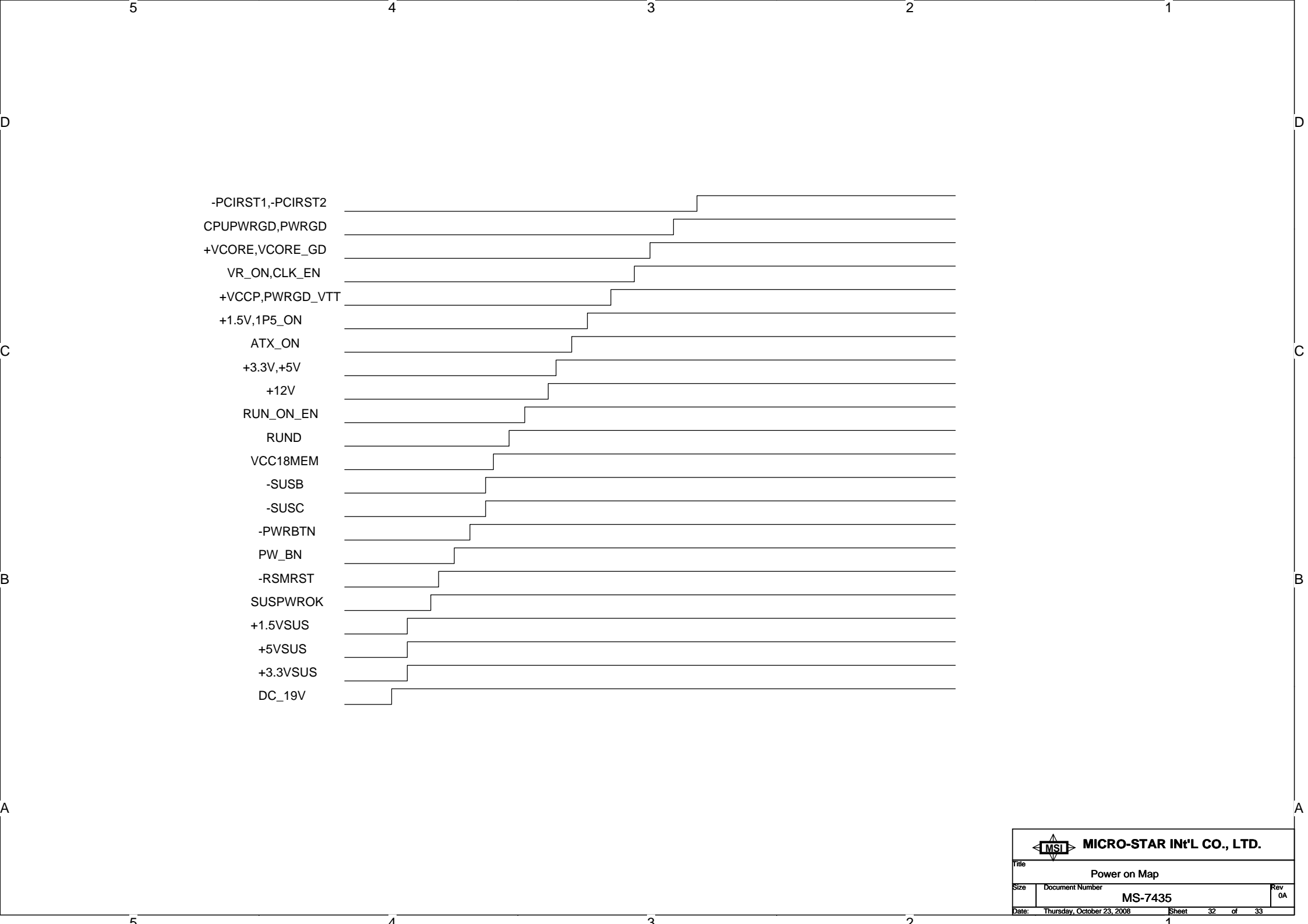
Top Layer

Int side



MANUAL PART





5 4

2008.9.8

1.VIA suggest :
(1) : -SERR & -DEVSEL need pull up 2.7K ohm to +5V
(2) : -TCS_EN Pull 4.7K to GND , pull high +3.3V做option.("0" Enable TPM "1" Disable TPM)

2.ADD Y5 Reserve for LAN 25MHz

3.eSATA Vendor suggest, reserve :
(1) 7707 and LDO co-layout
(2) EN signal of 7707 is active after 40ms when 3.3V power ok

4.ADD GPIO8 & GPIO9 test point

2008.9.9

1.ADD CR1 Pin4 +3.3V for MS-4177 Card Reader Controller

2.ADD -COMRST Reserve for COM Port

3.VIA Suggest : Change DIMM VDDSPD(+3.3V) pull up to VCC18MEM

4.Change PCI-e X4 to PCI-e X16

2008.9.10

1.Realtek Suggest:在有極性電容後面加上對地22k OHm 降低切換In/Out時降低POP Noise使用

2008.9.18

Change eSATA connector PN: ON5-7431003-F02 TX/RX

ISL9501 can support 19v directly due to ISL9501 is the Notebook power IC.
Just change 12in to 19v in
Change eSATA connector Part Number to N5N-07M0481-H06

2008.9.19

PM request :Remove SW1---0919

2008.9.22

Change JBAT1 PN to N32-1020900-H06,Change Battery to D06-0100300-K26

2008.9.23

Add Mini-PCIE Stand off E2B-1034010-L63

Change SATA Power connector N93-04M0281-H06 to N32-1040161-H06

Change VX800 heatsink to E31-0400641-K08

Change Y2 to D04-1001100-F07

Change Y3, Y4 to D04-0300800-T16

2008.9.24

Change VX800 heatsink to E31-0401600-K08

2008.9.25

Change COM Port to N32-2051651-H06

Change C216,EC8 to C51-107502E-A15、Add D17 for FAN

Remove TPS51125 EN0 control circuit

Reserve some decoupling CAP for CPU

2008.9.26

Change e-SATA U36 enable pin to 1.5V for RC delay 40ms

Repair DDR power and 1.5V output component

Change Power On sequence

Change EC1,EC2 to C71-221026E-S03

2008.9.27

Remove J2

2008.9.30

整合D4,D5,D6,D7 to D4 (PN:D0G-0422003-P03)

Change DVI F2 form 3.3V to 5V

整合DVI,VGA connector爲整體,PN:N58-39F0021-T05

2008.10.06

1.VIA suggest : If your CPU PWM is not CLK enable function pin.
=>We recommend the CLK enable pin connect 10k ohm to +3.3V directly.
Unmount Q25 and C481,R379

2.The Tx pair and Rx pair is reversal.
=> Please double confirm the symbol (MINI_PCIE1) is not wrong.

3.Please add level shift for SPD2/SPCLK2.

4.Please confirm U5 and U6 is TTL Level input (Change to T34-01G0809-T07)

3 2 1

5.Unmount R190

6.reserve pull high resistor 10k ohm to +3.3V.(TP15,TP16)

7.Change USB pin name to match USB Port

8.Reset Bottom is only active CPUPWRGD, but the PWRGD (SYSTEM) will not be active.
=>The Power GD circuit please reference VIA Demo board.

9.Please add 0.1u at PEX1RX+ and PEX1RX- near U12.(C481,C543)

2008.10.07

Schematic error , RN10 unmount ,RN11 mount ,Remove R79,ODTA3 link to RN11---1007

Change U35 to T39-01G0009-T07, Remove U34

2008.10.09

VIA Suggest:

1.The VCP port and COM port is multiple function and it is recognize which function is after Reset.
=>So, we recommend use "Reserve circuit for COM port" by default.
Unmount R132,R134
Mount U37,R428,C395,R332

2.If your USB Connector have Two Port USB and your Power used same Power
=>(1). You can disable Port 3 & Port 5 at same time when over current occur.
Because your Port 3 and Port 5 at same connector.
(2). Port 1 and Port 4 is same Power source, so their OC can connect to each other, too.

3.Reset seems is ok, but your Vcore _GD is not connect to this circuit.
=>it must mount R409 by default for save.
Ps: 1. Because, we worried about your Power GD circuit will fast then another Power.
2. Our Demo board doesn't used Vcore_GD by default.
=>Because, our power GD source is ATX_PG.
It is more delay then another power for normal.

2008.10.15

1.MINI_PCIE1 PIN 22 加一顆10P 對地電容,不上件預留

2.PCIE1 PIN A11 加一顆10P 對地電容,不上件預留 .

3.U14 pin 2 / pin 3 / pin 5 & J1 pin3 / pin4 接法有誤 ,請參考附件(SPI.pdf) U20 & JSPI1 .

4.U12 PIN 47加一顆10P 對地電容,不上件預留 .

5.EC12 不上件 , EC14 / EC17 上與EC15相同即可 .

6.USB 是否要過訊號量測 ? 若要過則要上COMMON CHOCK .


7.C453 / C459 / C454 / C455 / C472 / C473 / C474 / C475 / C476 / C477 / C478 / C479 / C480 / C508 要上25V 以上的電壓值 .

8.C505 / C507要上16V 以上的電壓值 .

9.Q5,Q7 改用SOT-89 OR S08 之 P-MOSFET SOT-23 很容易燒燬

2008.10.22

J1,PCIE1,IDE1在限高區,0A先不上件

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